Nordcad

High-Speed Design and Simulation

Agenda

- Part 1
  - High Speed Design – what exactly classifies as high-speed
  - When is signal integrity good enough? An introduction to noise budget
  - What to do at what stage in the design cycle
- Part 2
  - Model extraction
  - Different approaches to memory simulation
  - What is so special about serial interface simulation

Introduction

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- Who am I?

- Introduction to Nordcad
  - Cadence Channel Partner in Nordic countries
  - Schematic, PCB, Circuit Simulation, CAD/CAM, RF/MW simulation, Signal- and Power Integrity, Thermal simulation, CFD, Meshing, PLM and services
  - 20+ employees, sales and technical support
  - Headquarters located in Aalborg Denmark
  - Office in Stockholm Sweden

Part 1

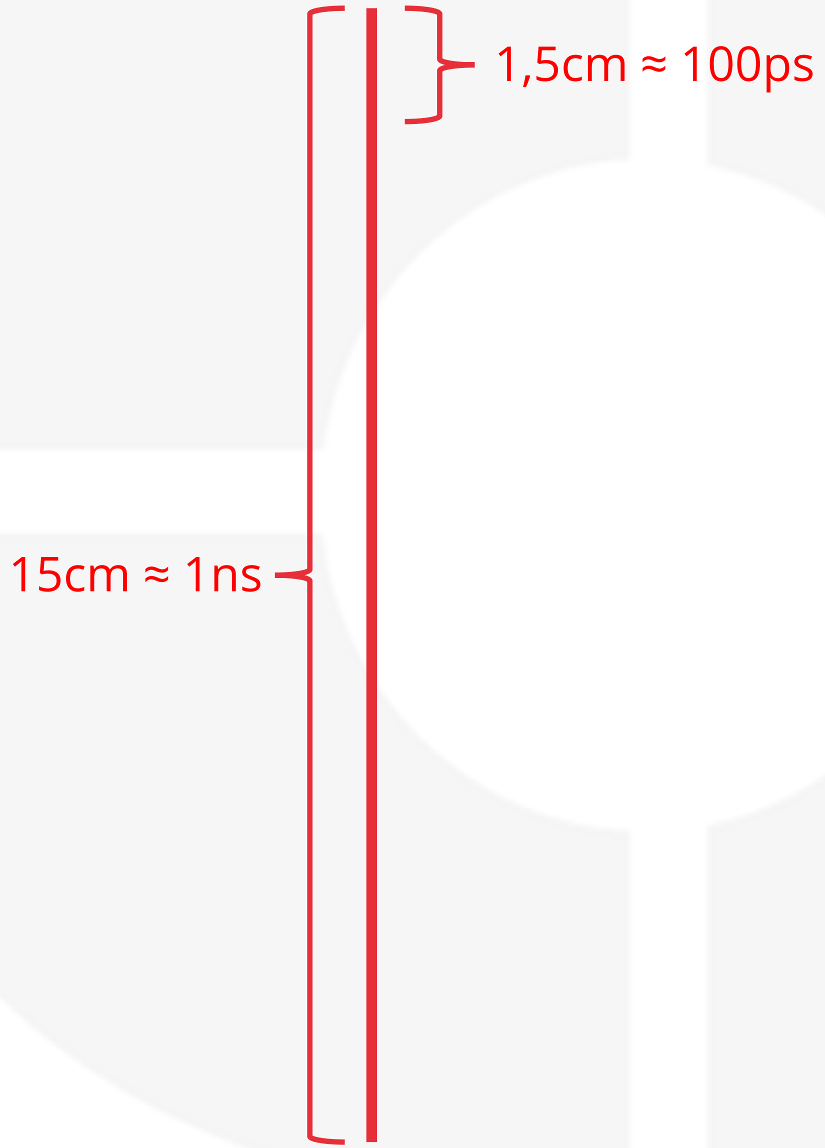
High-Speed Design

What classifies a design as high-speed?

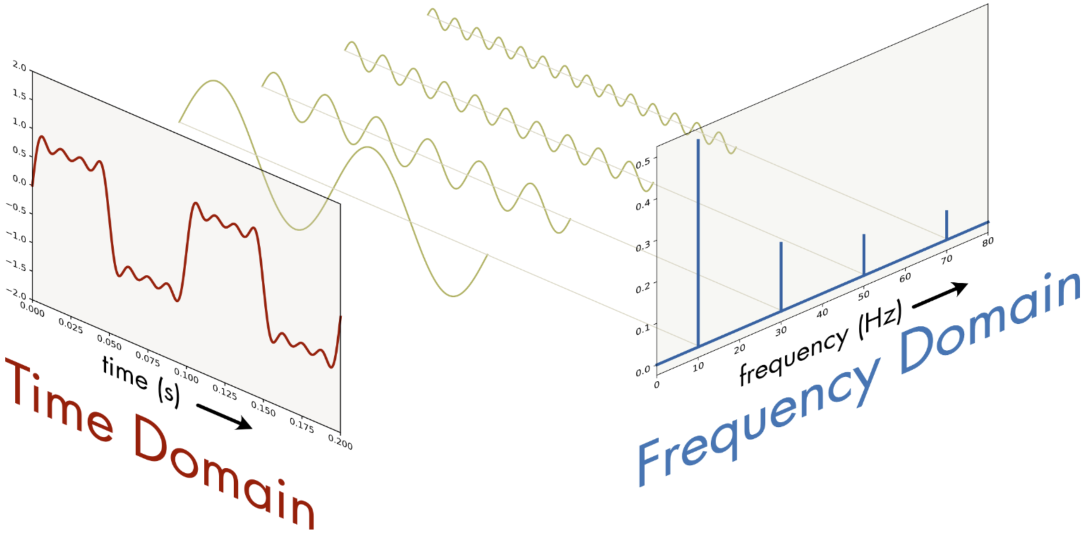
- Fast clock speeds?
  - 50MHz?
- DDR memory?
  - DDR?
  - DDR5?
- Serial links
  - Fast Ethernet 100Mb/s?
  - Gigabit Ethernet 1000Mb/s?
  - PCIe?
  - HDMI?

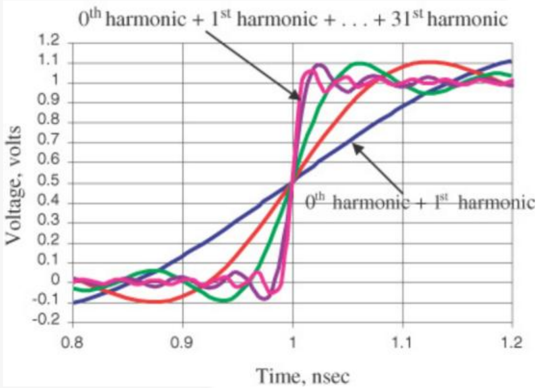
Transmission lines

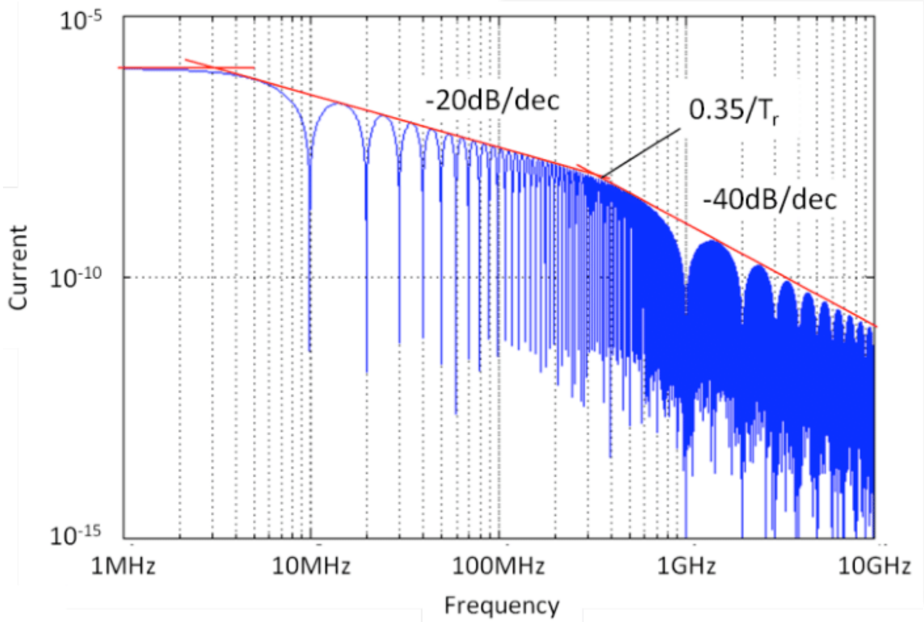
- High-speed is always related to the signal rise time t_{rise}
- Signal reflections start to occur when transmission lines are $\frac{t_{rise}}{2}$
- Signal crosstalk start to occur when transmission lines are $\frac{t_{rise}}{4}$, so half of the limit for reflection
- Back in the day high-speed interfaces utilized high-speed drivers, but today most drivers have sub 300ps rise times



Square wave signals

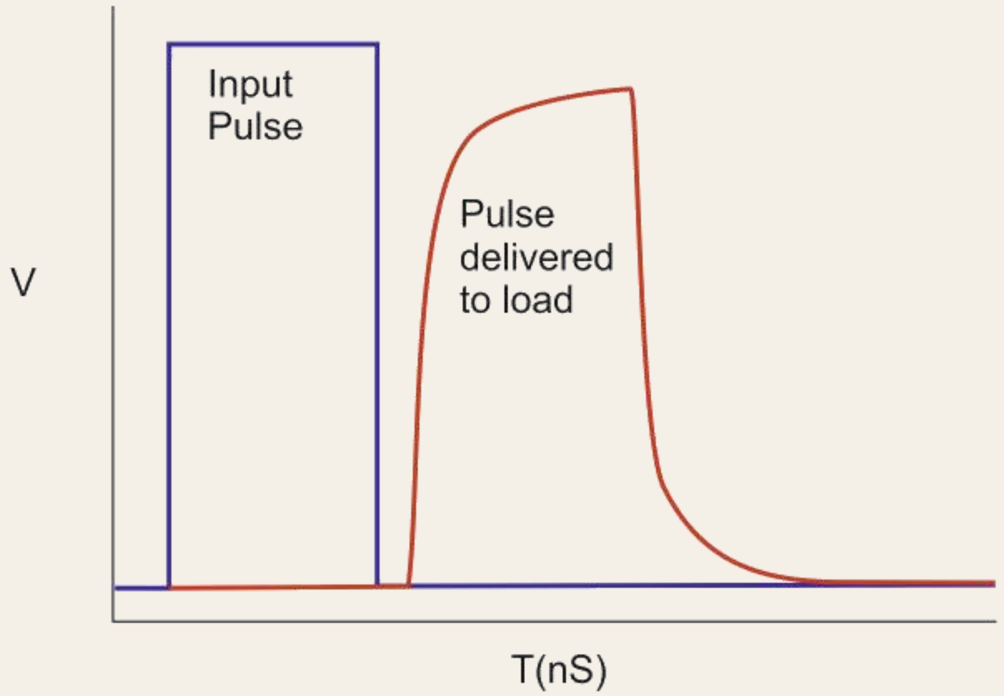


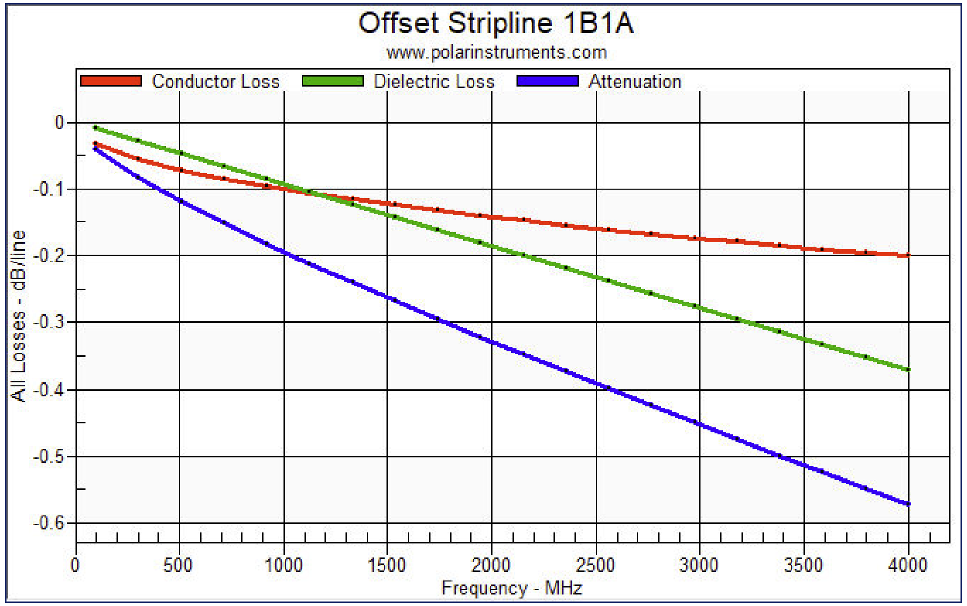




Signal integrity in a nutshell

- Input signal with given frequency content, amplitude and phase to transmission line

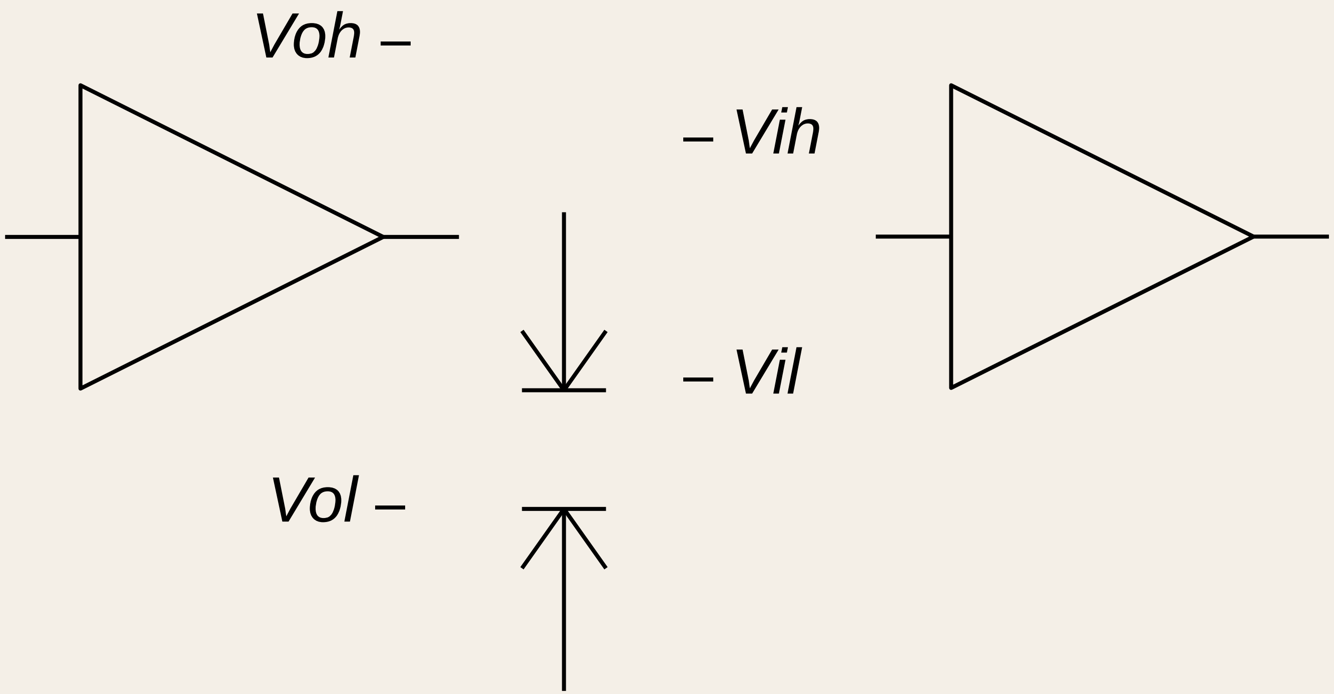




- Receive signal with same frequency content, amplitude and phase in receiving end

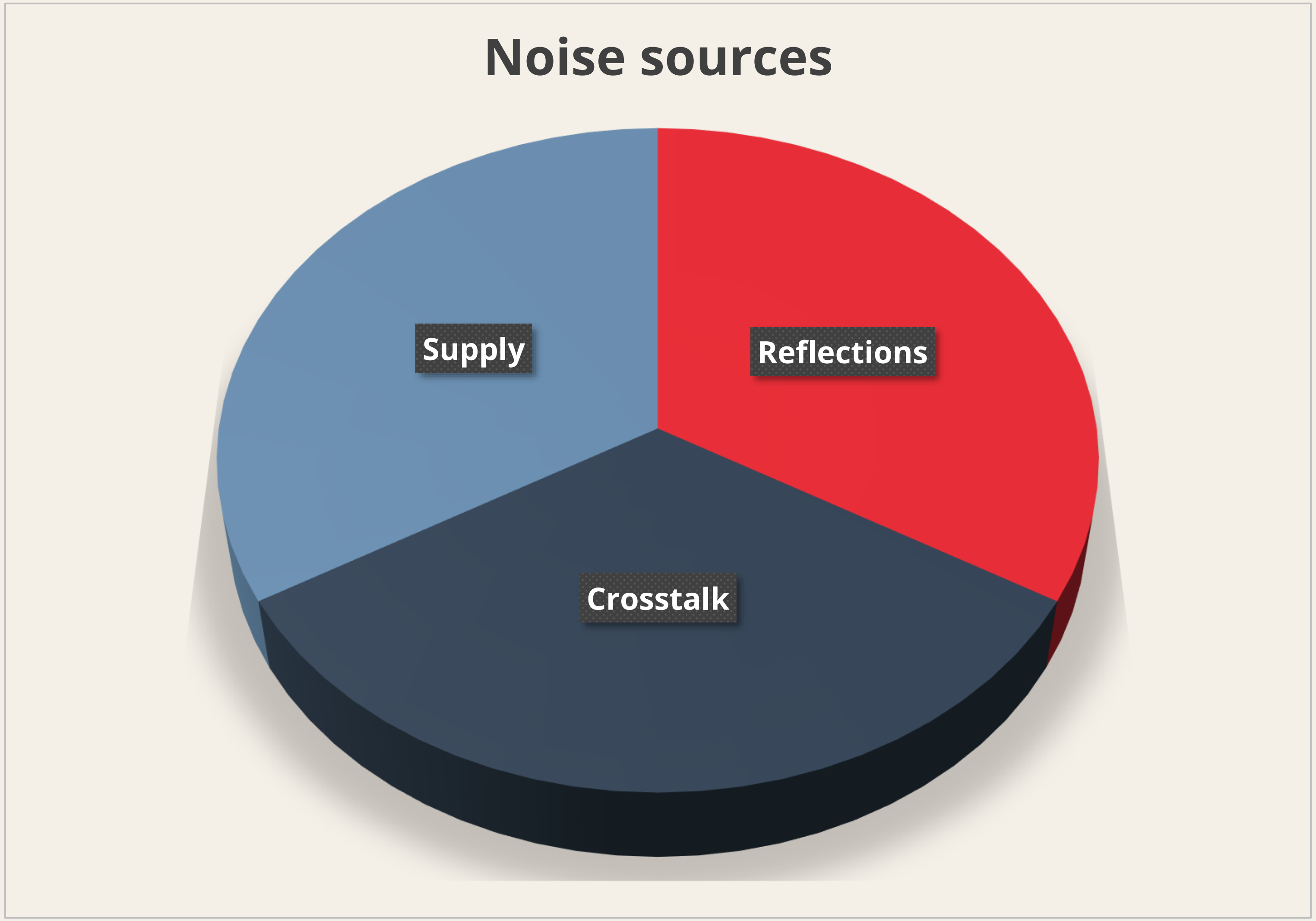
Introduction to noise margin

Noise margin



Noise Margin = Vol-Vil
(or Voh-Vih)

Largest noise sources in digital circuits

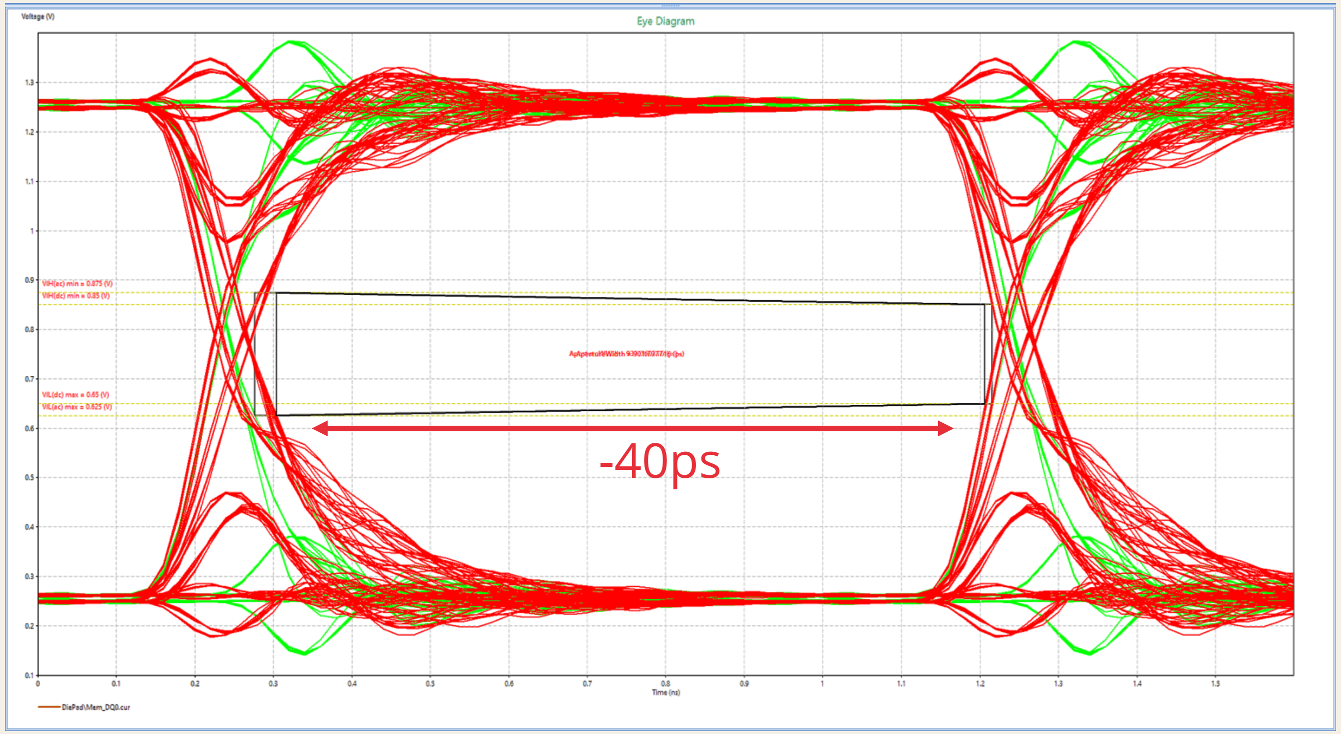


Reflection

Impedance and Terminations

Trace impedance

- Why is it interesting to minimize impedance mismatch?
  - Seen through Signal Integrity glasses it can have a great impact on performance



Minimizing reflections

- Reflections are caused by impedance mismatch
  - Trace impedance mismatch
  - Improper termination

- Trace impedance is driven by fabrication and yield
  - Tolerances on transmission lines

- Proper termination required for modern high-speed circuits
  - Termination type
  - Termination placement
  - Termination value

Reflection - termination

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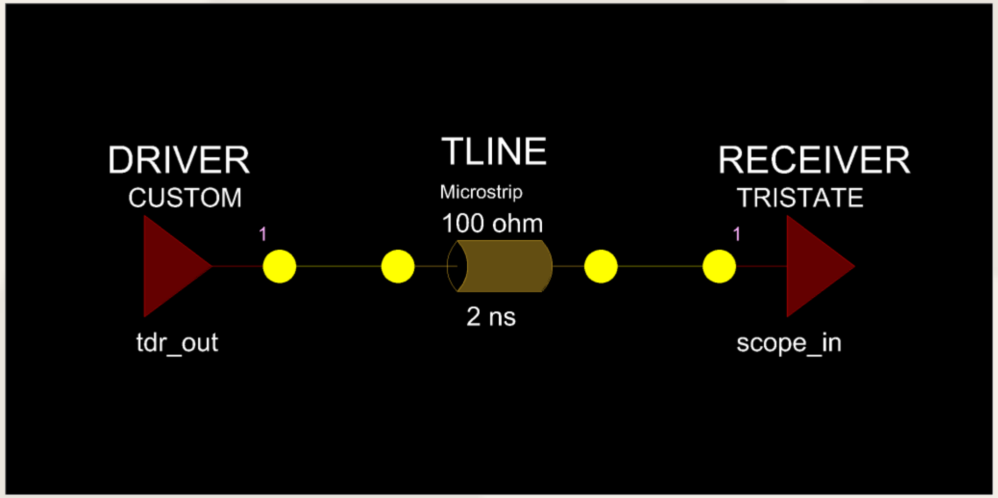
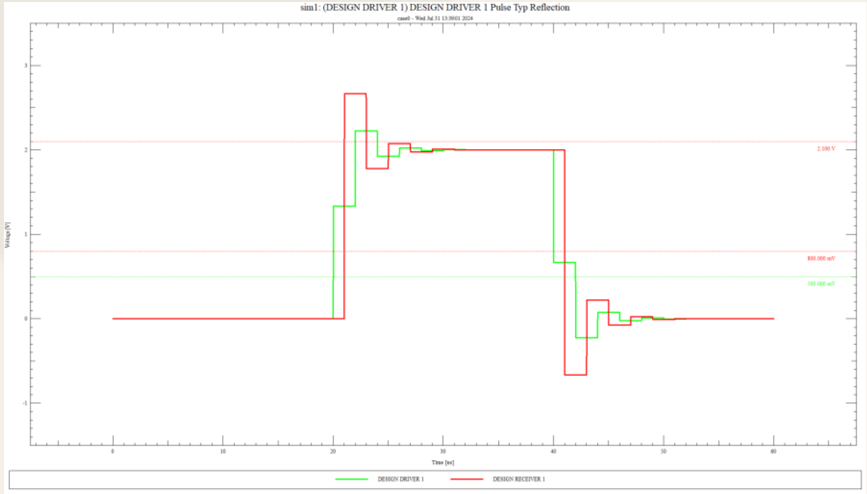
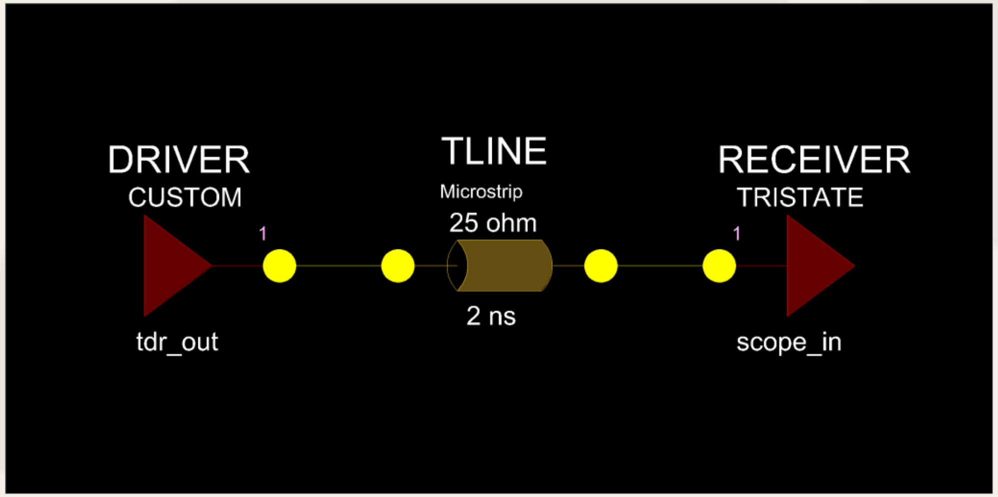
- Poorly matched impedance
  - Too low impedance entering transmission line
- Overshoot which might break receiver over time
- Reflection noise eats noise margin

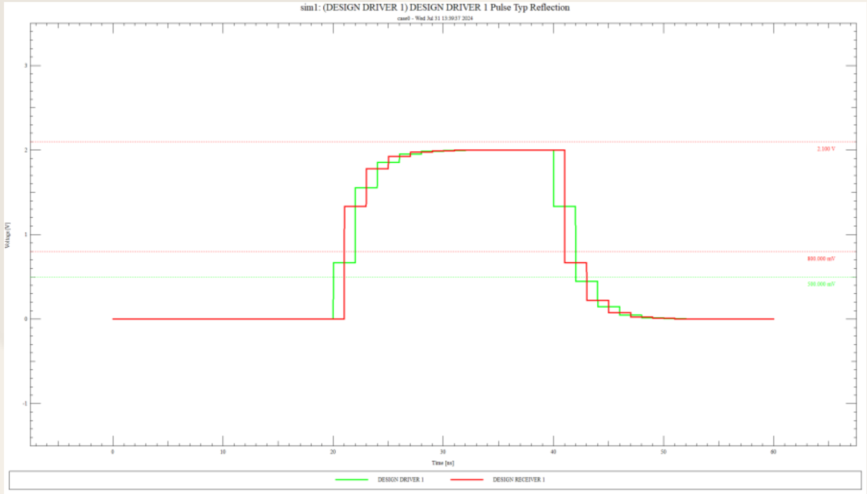




Reflection - termination

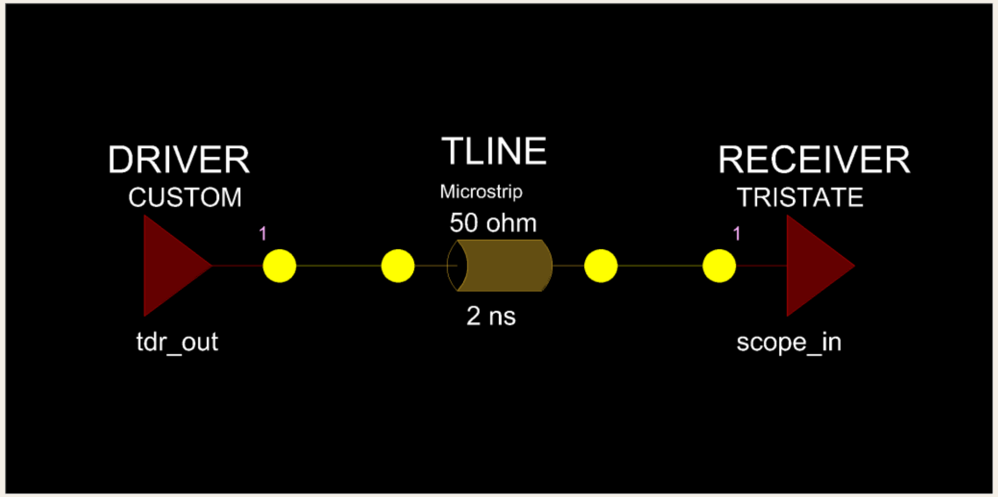
- Poorly matched impedance
  - Too high impedance entering transmission line
- Multiple roundtrips before steady-state voltage
  - Decreased timing
- High current consumption required for driving transmission line

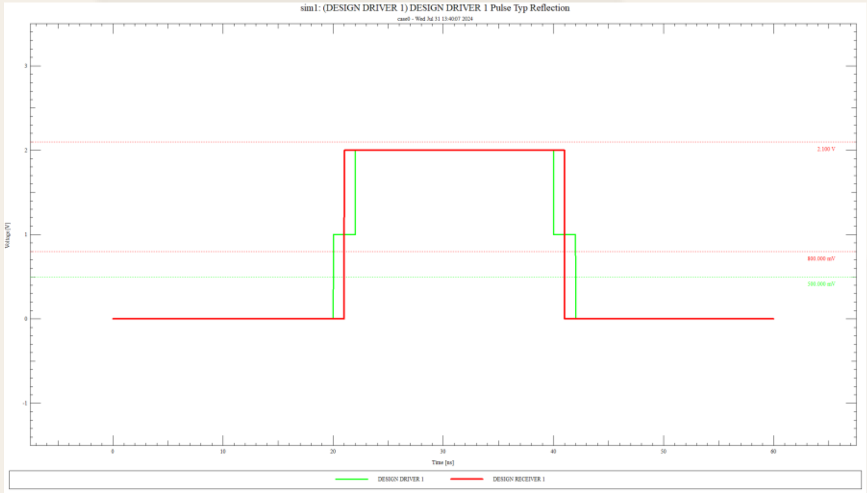




Reflection - termination

- Perfectly matched impedance
- Voltage entering transmission line is half desired voltage





Series termination

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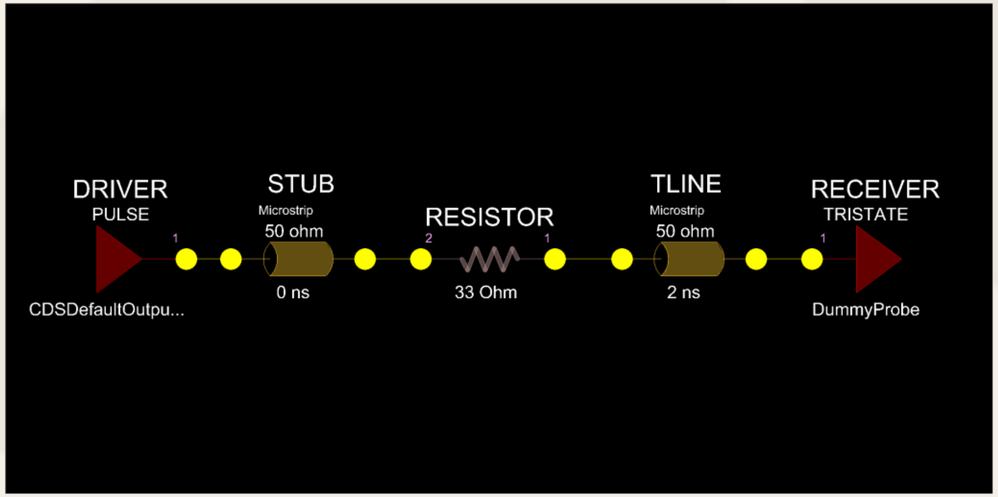
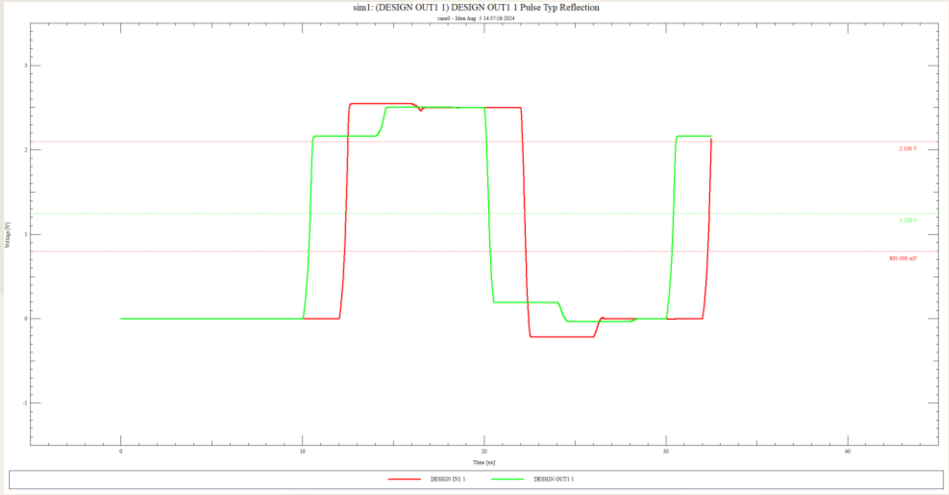
- Reflection mode switching
- Very good for one direction point to point connection
- No requirement for strong drivers
- Effectiveness relies on how close it is to the transmitter
- Output impedance for rising and falling are seldom equal





Series Termination Stub

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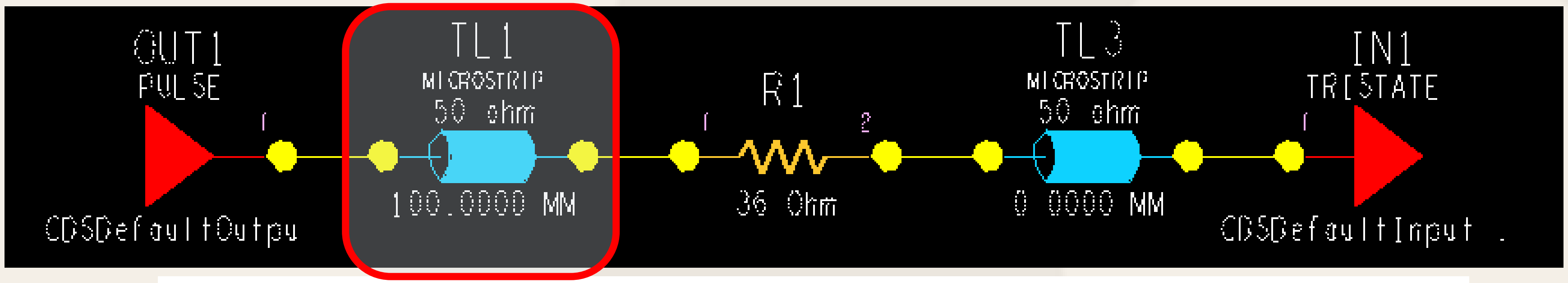
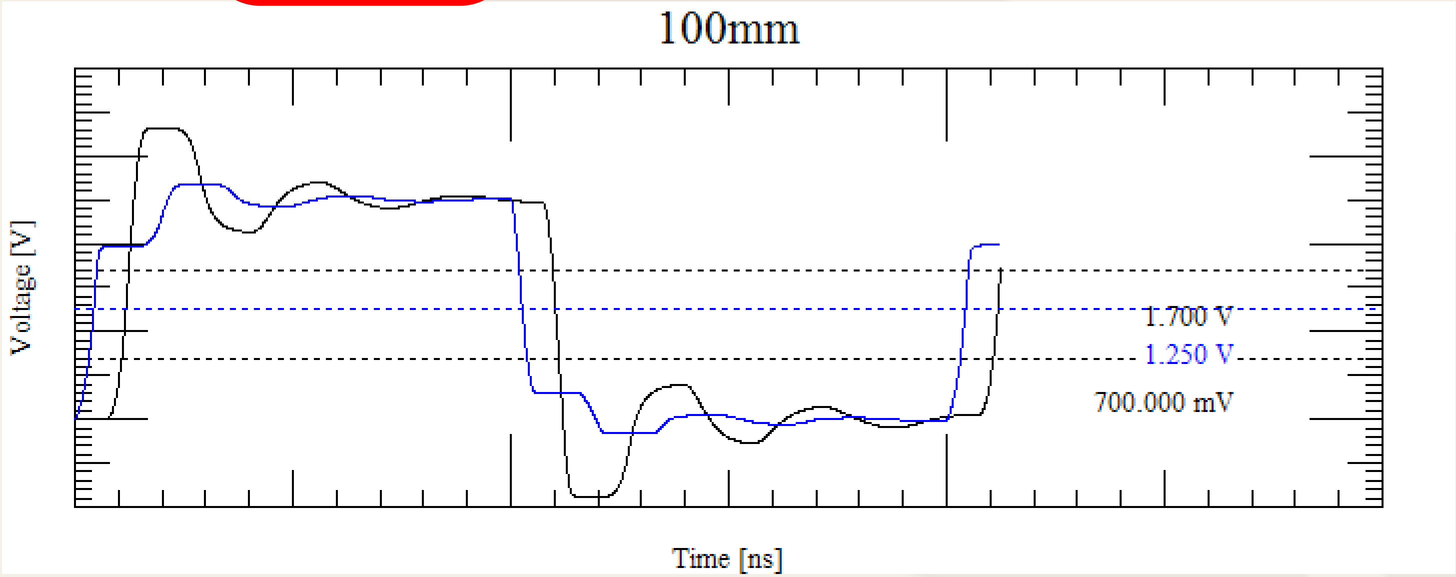
- Placement of series terminator has great impact of its effect
- Animation where terminator is moved along 100mm transmission line in 10mm increments
- How long a setries termination stub is allowable?

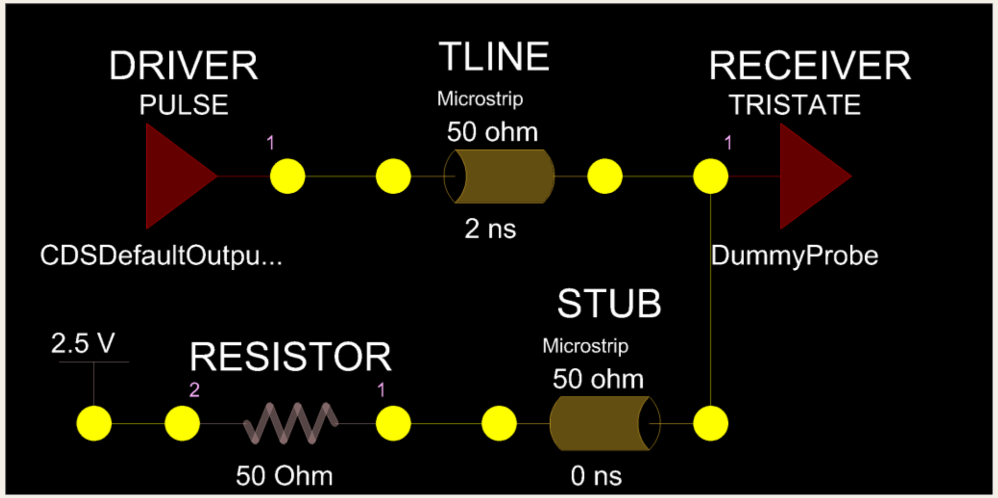
Series Termination Stub

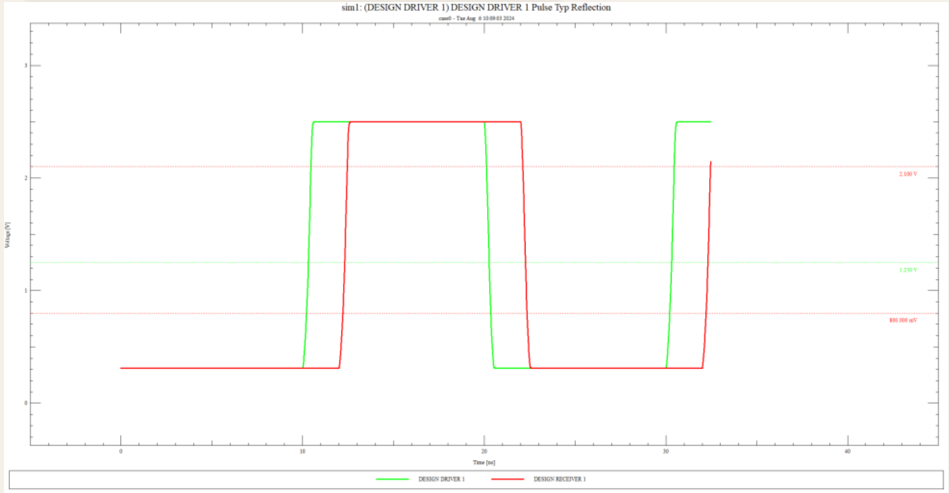




Parallel termination

- Parallel termination impacts voltage swing
- Has increased current draw
- Ideally must be the last element on the lines
- Stubs change performance



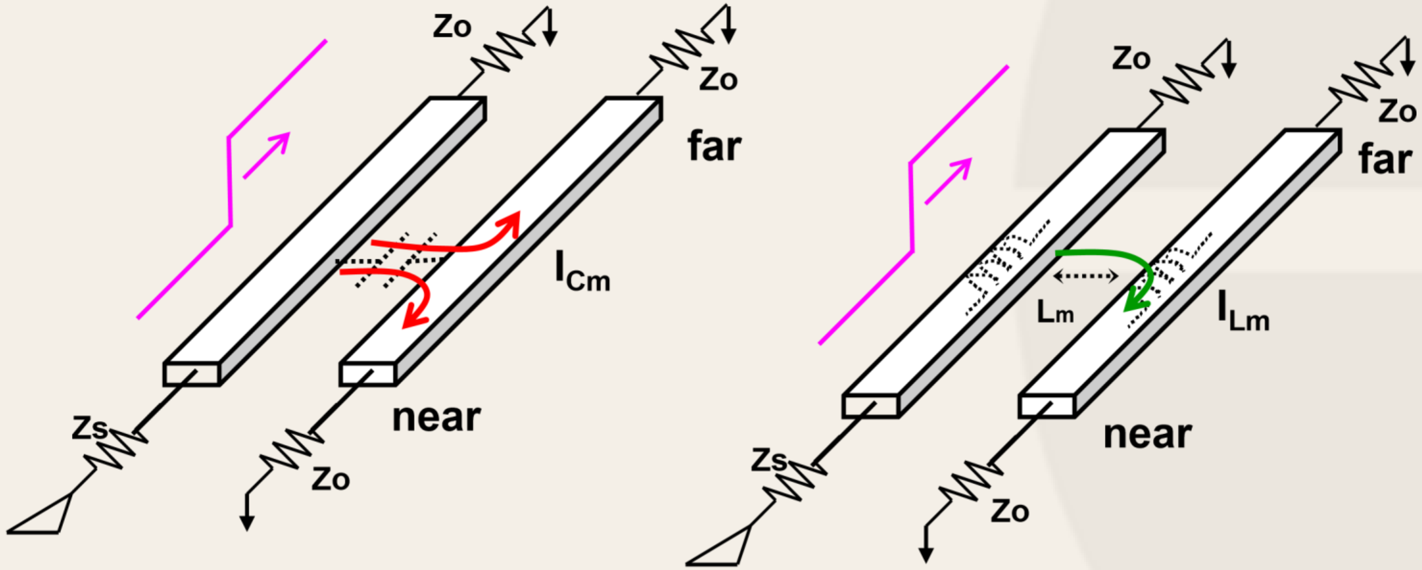


Crosstalk

Coupling

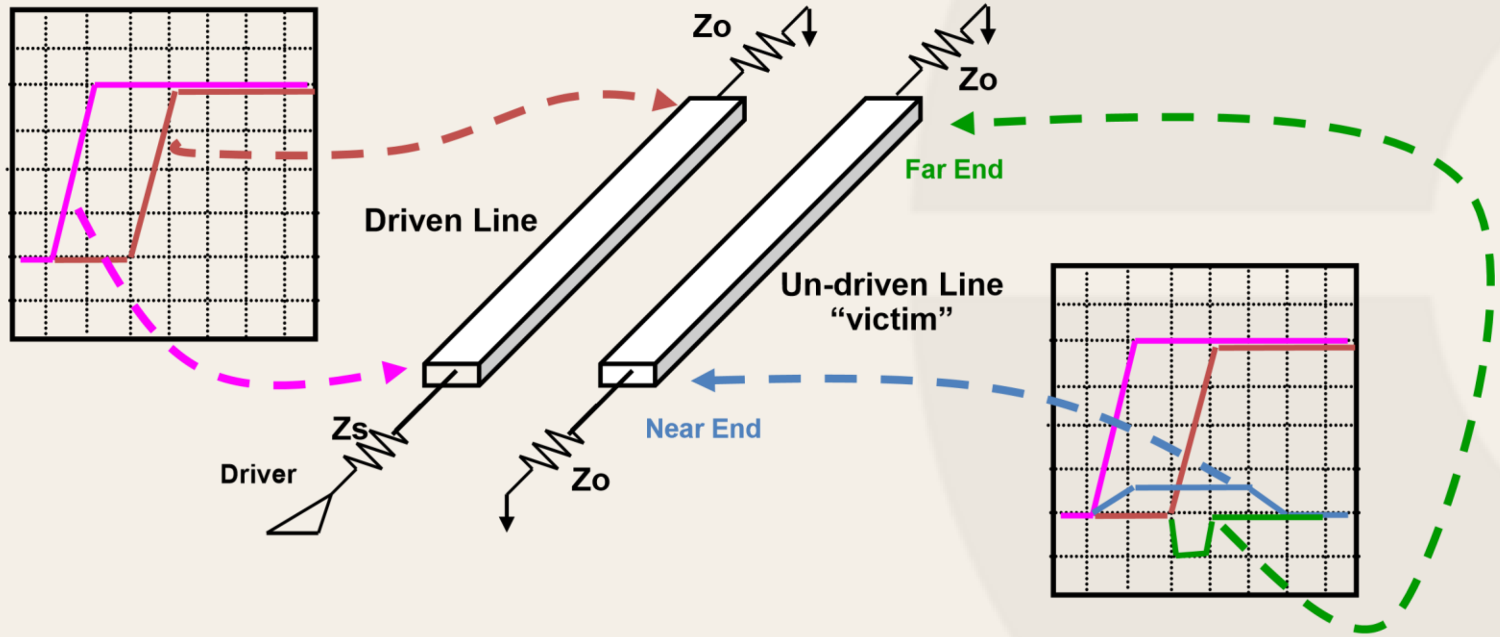
Coupling

- Coupling arises from mutual capacitive and inductive coupling between traces

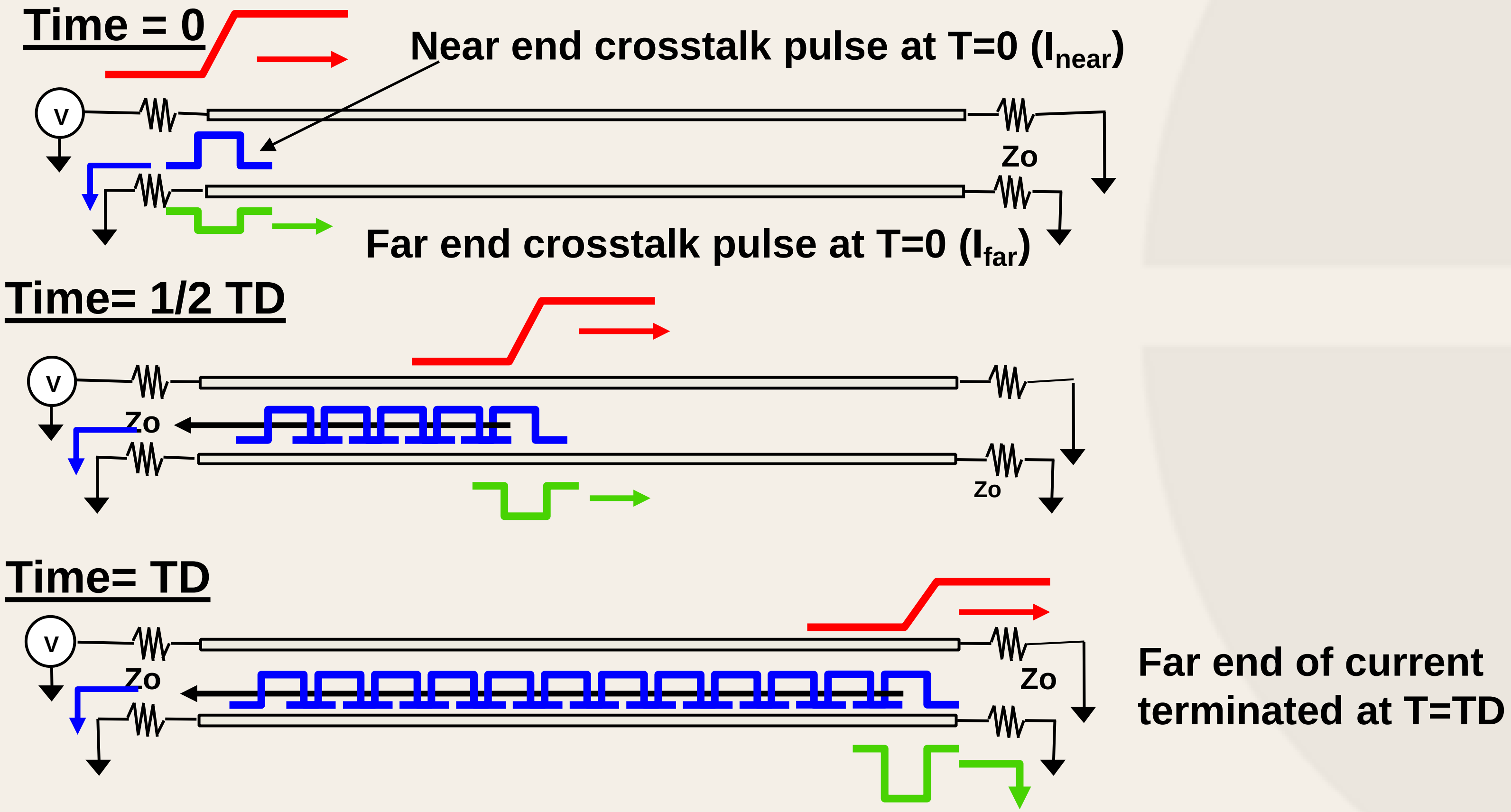


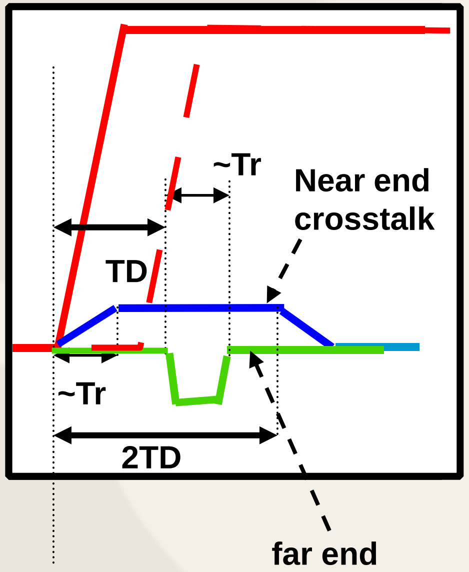
$$I_{near} = I_{Cm} + I_{Lm} \qquad I_{far} = I_{Cm} - I_{Lm}$$

Coupling and Crosstalk



Coupling and Crosstalk





Simulating Crosstalk

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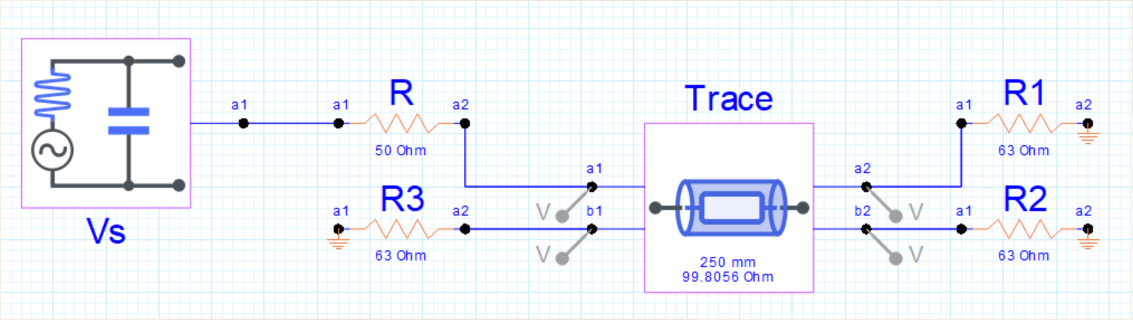
- Topology consist of two nets
  - Aggressor
  - Victim



- Victim is parallel terminated to minimize reflections

- Near end crosstalk will in most PCB designs be the one to manage

Trace spacing

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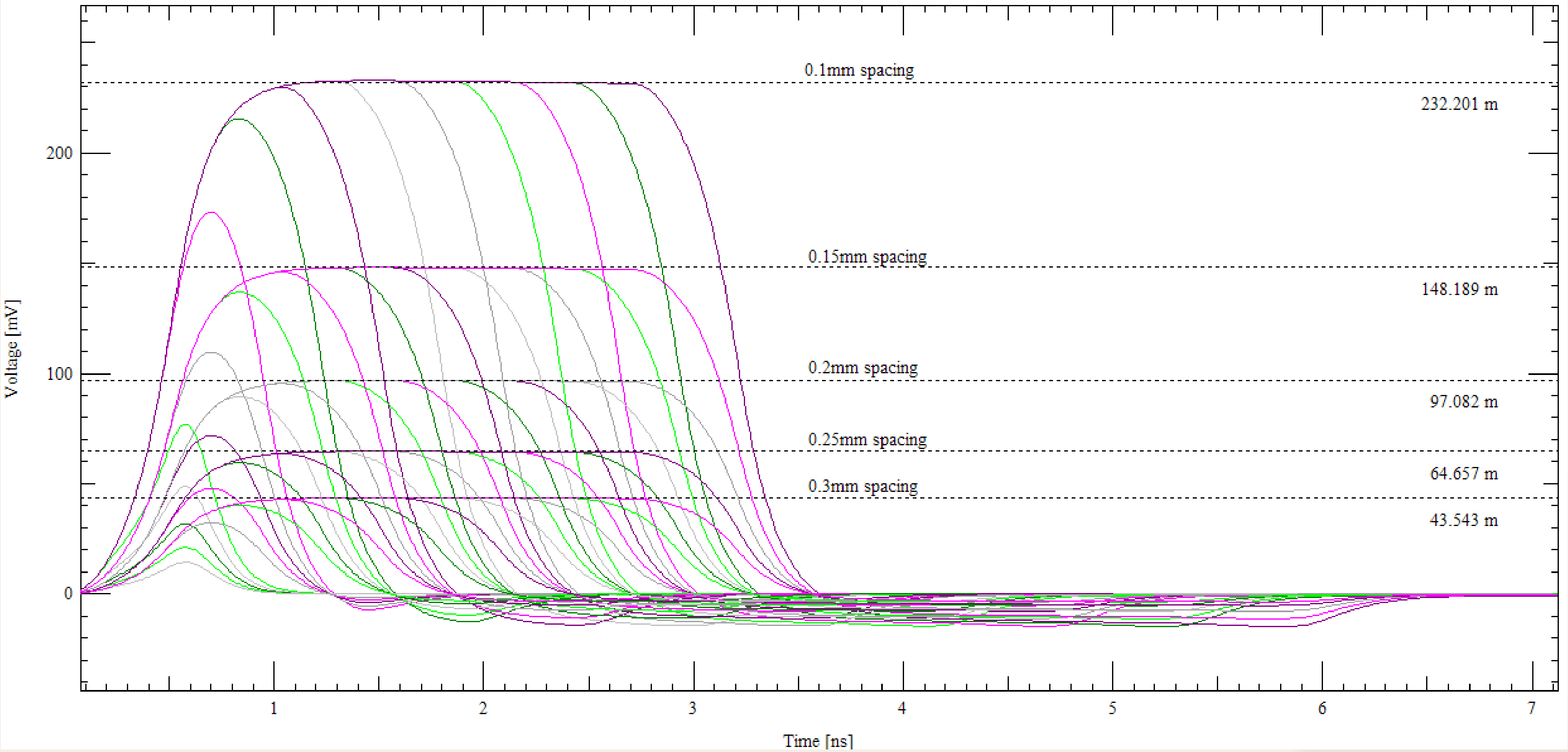
- Spacing between traces and length of parallel routing



Stackup parameters

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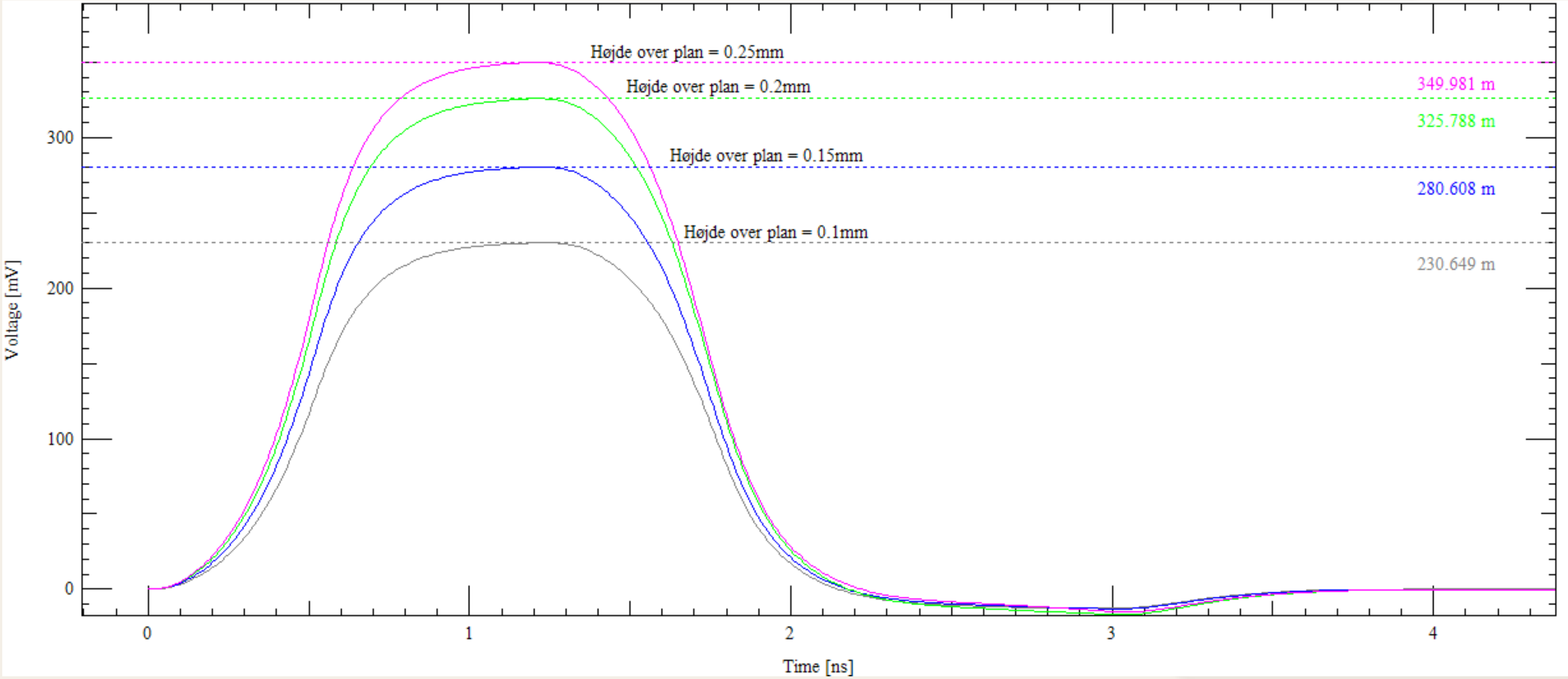
- Distance between routing layer and reference layer



Design cycle

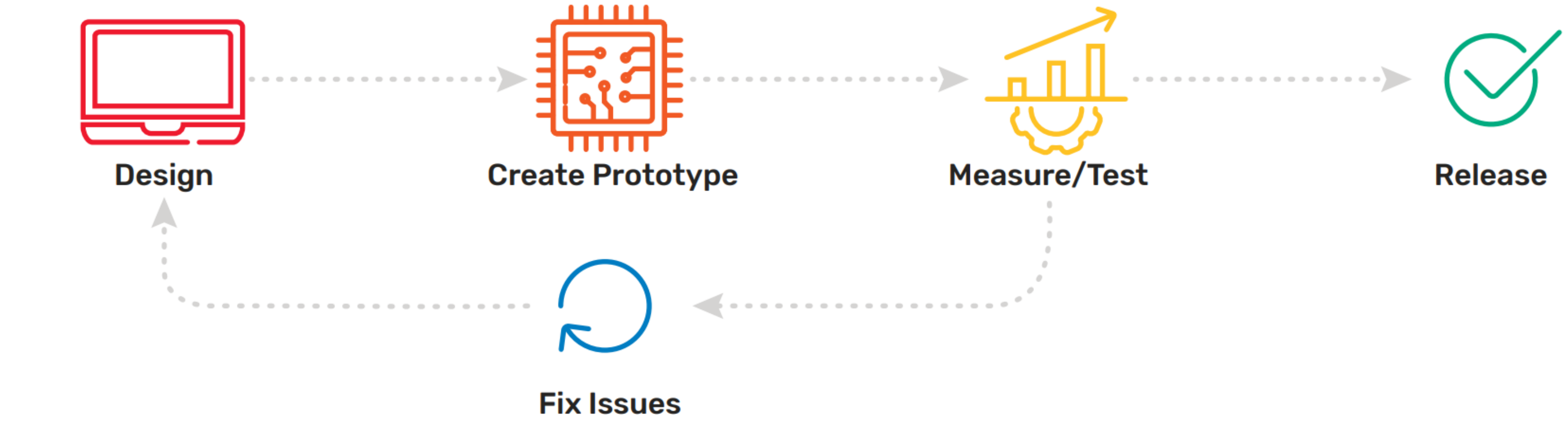
- Easy and straightforward flow
  - Very uncommon but great starting point

Part 2

High-Speed Simulation

Simulation driven flow

Traditional Design



Simulation-Driven Design

Model Extraction

Model extraction

- What needs to be captured for “good” models?
  - Impedance
  - Coupling
  - Return path
  - Losses
  - PDN

- Do we need to correlate with measurements?
  - Of course, but set expectations accordingly!
  - And use similar behavior as simulation

Model extraction

- Understand limitations of your extraction engine
  - What features are supported, and which aren't?
  - Is there a frequency limitation?

- Does the extracted model work for the given analysis?
  - S-parameters can be difficult in time-domain
  - Spice based models are fast

Topology extraction

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- Single net mode
- Captures
  - Impedance
  - Length
  - Logical view of routed net
- Great for constraint development

Spice model extraction

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- Single or interface extraction
  - Lumped spice model
  - Time domain models
  - FDTD is even an option for power-aware simulation
- Captures
  - Impedance
  - Coupling
- Fast and easy for time domain simulation
- Great for understanding impact of trade-offs during routing

S-parameter extraction

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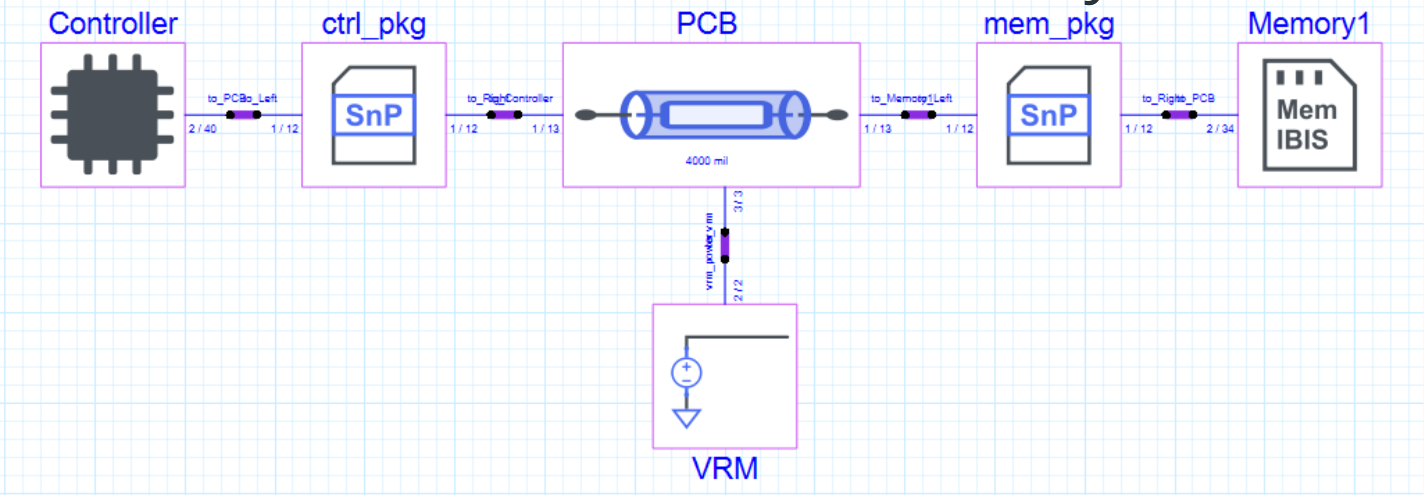
- Single net or interface
  - Frequency domain models
- In theory, captures everything!
  - Impedance
  - Coupling
  - Return path
- Different solver technologies (multiple vendors)
  - Hybrid solver – faster and easier, limited capture
  - Full wave 3D – slower and more complex, captures everything
- Great for final verification

Memory interfaces

Different approaches to simulation

Will it work or not simulations

- What is required for that kind of analysis?
  - IBIS models with defined power rails
  - Extracted layout model
    - Interconnect model including PDN with capacitors – derated of course ☺
  - Package parasitic models
  - Die and package decoupling
  - Timing parameters for controller and memory



Different analysis approaches

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- Will spice extraction with generic models capture uncertainties?
  - Doesn't require a lot of experience
  - Fast and easy to debug

- What does addition of IBIS models add to the above?
  - Better voltage levels, currents and load impedances
  - Package parasitic and capacitance

- Does frequency domain interface models enrich your analysis?
  - Adds power domain to simulations
  - Review interface through s-parameters
  - Captures more details

Serial Links

Channels and Analysis

Serial links

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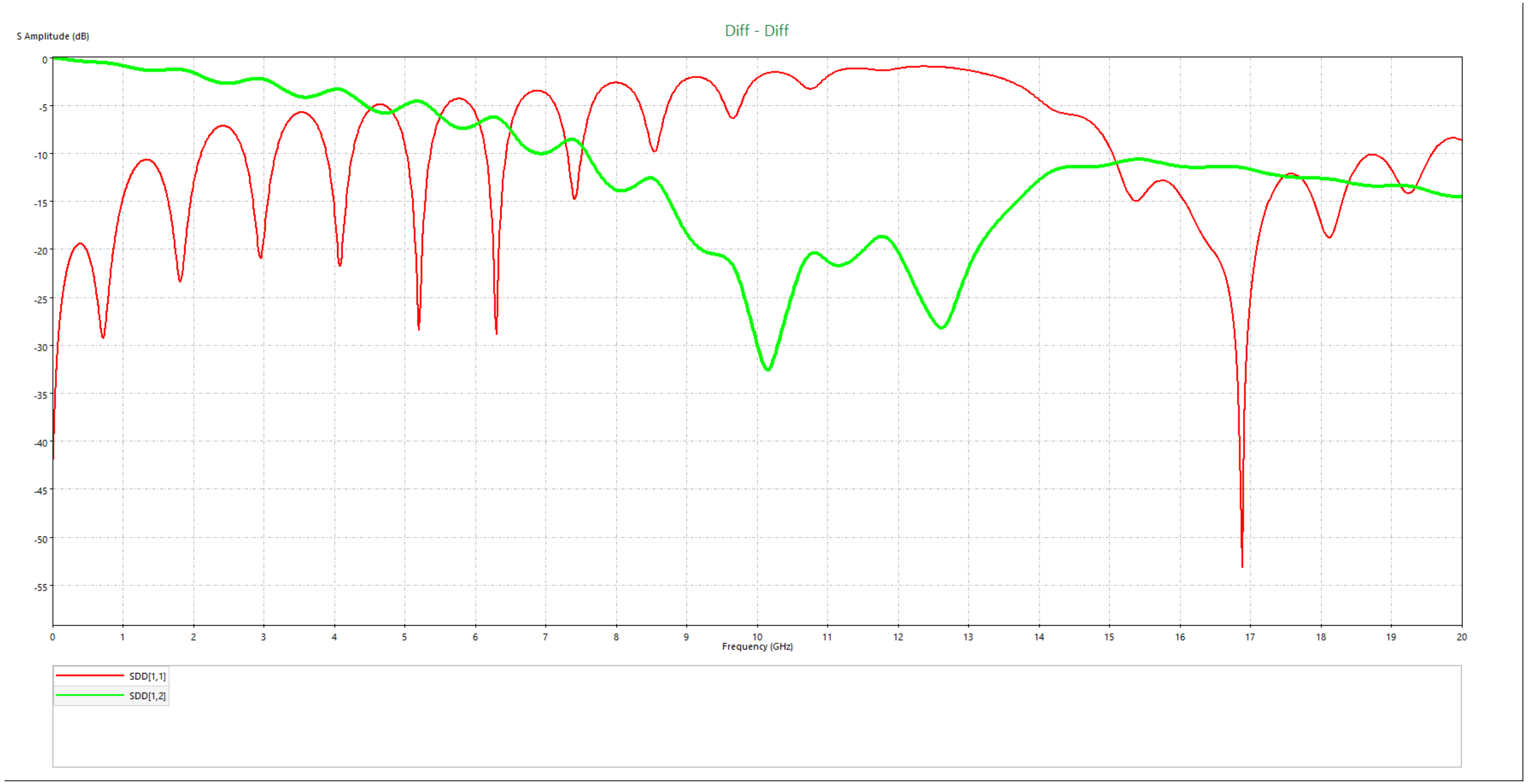
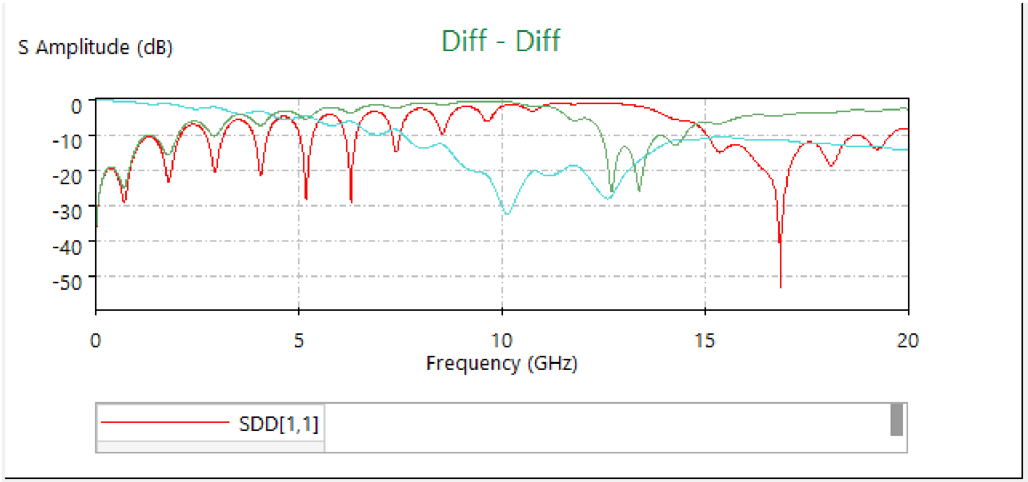
- Simulation of serial links requires s-parameters
  - Depending on speed and layout structures 3D full wave extraction is often required
- Some interfaces can be analyzed by s-parameters and doesn't require simulation
- Simulation of serial links often relies on IBIS+AMI models which describes IO plus clock and data recovery
  - Methodology we also see in newer memory interface simulations

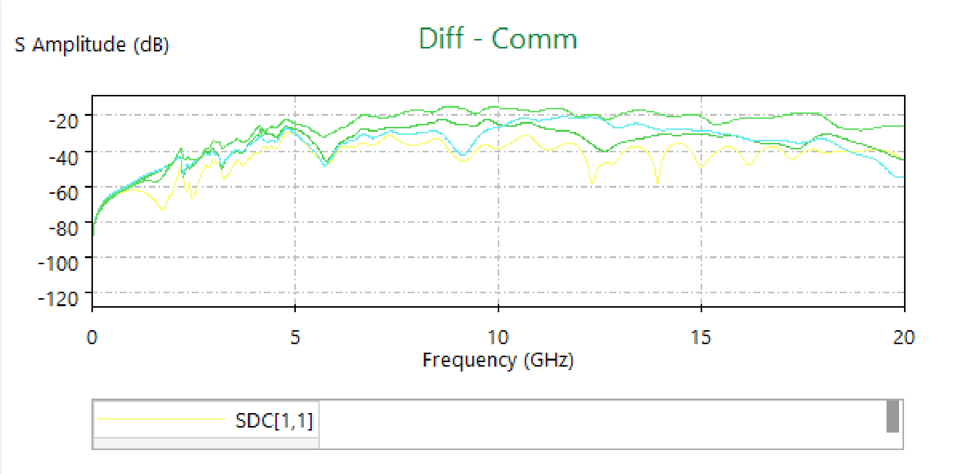
Insertion and return loss

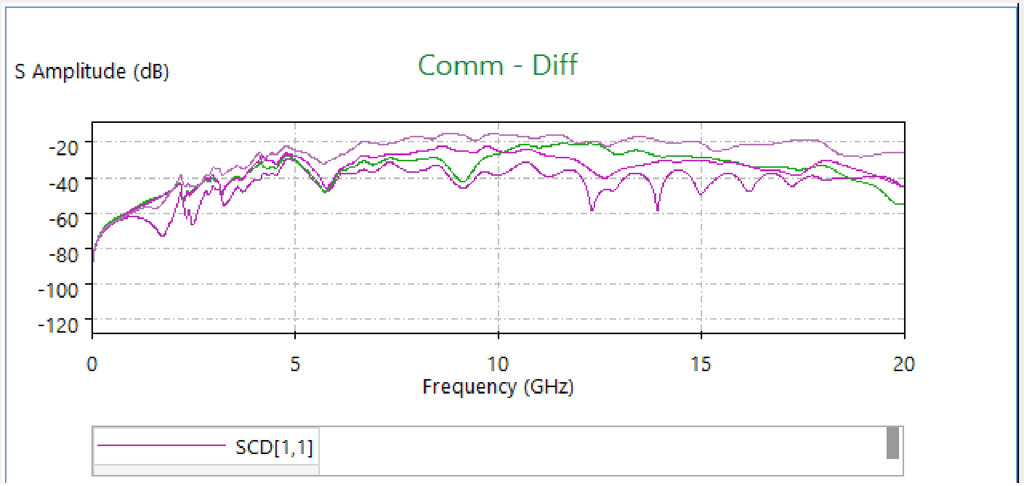
- Main goal for differential channel is to keep insertion loss high and return loss low

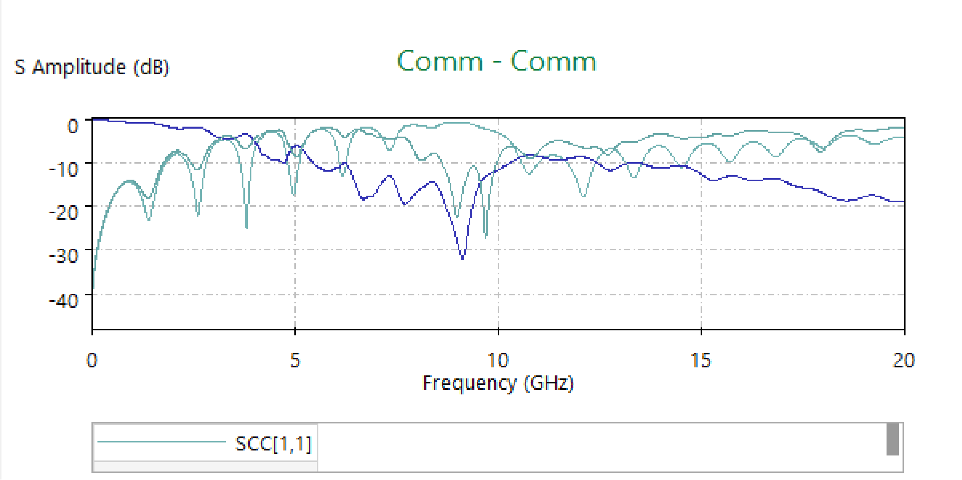


Differential mode s-parameters









Mode conversion

- 1st quadrant, EMI susceptibility
  - For perfect symmetric differential pairs numbers here should be low
- 3rd quadrant, EMI emission
- Adds distortion to differential signal
  - Reduced differential signal
  - Common mode signal may cause increased asymmetric noise
  - Common mode signal on cables may add to EMI
- Reasons for mode conversion
  - Difference in single line impedance
  - Length difference without compensation
  - Added elements to nets such as test pads
  - Return path issues
  - Fiber weave effect

Serial link simulation

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- Channel characterization
  - Step response
  - Impulse response calculated from step response
  - Impulse response modified with AMI

- Convolution and millions of bits
  - Simulation is different from regular time-domain analysis

- Eye width, height, BER and bathtub curves

Summary

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- Use analysis early in the design process (shift left)
  - Catching bug early is cheaper and easier
- Entry level tools are easier to come by
  - Tools are bundled with PCB tools and lots of free tools are available
- Don’t expect to analyze everything in first go
  - Partitioning your design and running analysis on all groups take time
- Correlation between simulation and measurement is difficult
  - Often verification doesn’t provide any real value