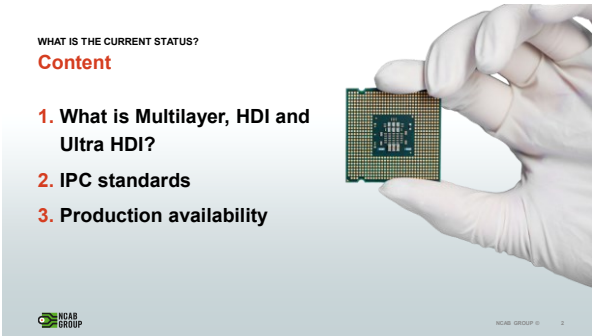


1



2

1. WHAT IS MULTILAYER, HDI AND ULTRA HDI?

What are the differences between these PCBs?

UHDI vs HDI vs Multilayer PCB

PARAMETERS	MULTILAYER	HDI	UHDI
Line/Space	> 75 µm	> 50 µm	< 50 µm
Laser drilled holes	No	Yes > 75µm Φ	Yes, < 75µm Φ
Mechanical holes	Yes > 150µm Φ	Yes > 150 µm Φ	No (?)
BGA pitch	>500 µm	>350 µm	< 350 um
Typical layer count	4->50	4->50	1-8
Dielectric Thickness	>90 µm	50 -100 µm	< 50 µm
Standards	IPC-6012 IPC 2226	IPC-6012 IPC 2226	IPC-2229/6019 TBA

3

INTRODUCTION TO MULTILAYER PCB'S

What is a multilayer PCB?

> Three or more conductive layers of copper which have been bonded to non-conductive substrates, yet are electrically connected where needed, so that they connect specific components using features (tracks and component pads) that have been imaged and etched to form a **bespoke design**, in order to fulfill a **bespoke function**.



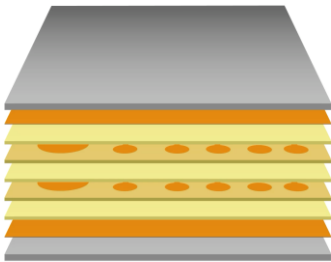
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LAMINATION 3.2

Lay-up

Steel plate
Copper foil
Prepreg
Inner layer
Prepreg
Inner layer
Prepreg
Copper foil
Steel plate



NCAB
Unique

NCAB ADDED VALUE
We only allow
the factories to
use materials
that comply with
IPC-4101

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Pre production	1.1 Engineering	1.2 Material issue			
Inner layer	2.1 Image transfer	2.2 Develop (Dry Strip)	2.3 AOI		
Lamination	3.1 Stack-up	3.2 Layer	3.3 Bonding		
Drilling	4.1 4-Step drilling testing holes	4.2 Mechanical drilling			
Plating	5.1 Desmear and electroless plated through hole	5.2 Solderable copper plating			
Outer layer	6.1 Image transfer	6.2 Developing	6.3 Reflow plating	6.4 Strip (Dry Strip)	6.5 AOI
Soldermask	7.1 Ink hole treatment	7.2 Printing and pre-cure	7.3 Exposure	7.4 Developing	7.5 Final cure
Legend	8.1 Printing and cure				
Surface finish	9.1 ENIG	9.2 Immersion Tin	9.3 100%		
Profiling	10.1 4-Step	10.2 Bonding			
Quality control	11.1 Electrical test	11.2 Final inspection	11.3 Final quality control		
Packaging	12.1 Wrap and pack				

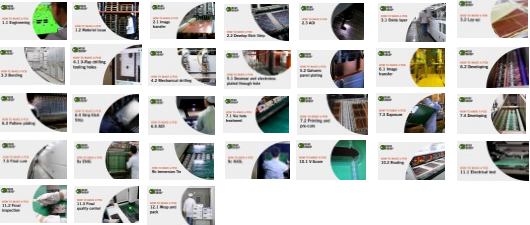


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INNER LAYER

Watch all Multilayer Production videos here





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Multilayer Design Guideline

PCB design guidelines
(printed circuit boards)
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1. WHAT IS MULTILAYER, HDI AND ULTRA HDI?

HDI and Micro via Criteria

Definitions:

High Density Interconnect

IPC-6012F defines HDI as a design with an average of **20 electrical connections/cm2** on both sides of the printed board.

These designs typically have **vias $\leq 150\text{ }\mu\text{m}$ / 0.006 in**, conductor **width and spaces $\leq 100\text{ }\mu\text{m}$ / 0.004 in**, **vias in SMT pads**, and/or where micro vias are employed



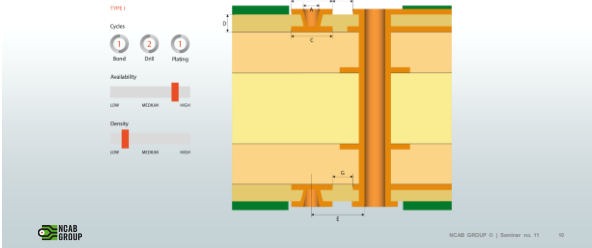
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WHAT IS A HDI PCB?

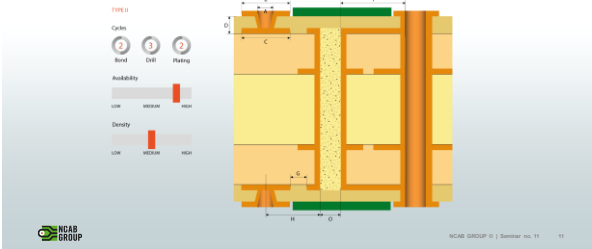
IPC-2226 Type I



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WHAT IS A HDI PCB?

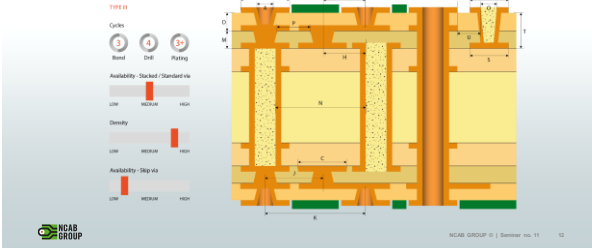
IPC-2226 Type II



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WHAT IS A HDI PCB?

IPC-2226 Type III



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HDI Design Guideline

PCB design
guidelines (printed
circuit boards) |
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HDI DESIGN GUIDELINES 1.2



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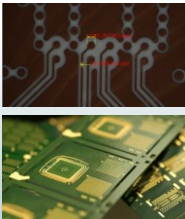
WHAT IS: ULTRA HDI, IC SUBSTRATE, SLP?

What is Ultra HDI PCB?

- > Products with lines and spaces below 50 microns
- > Dielectric thicknesses below 50 microns
- > Micro via diameters below 75 microns
- > Product attributes beyond the existing IPC 2226 Level C



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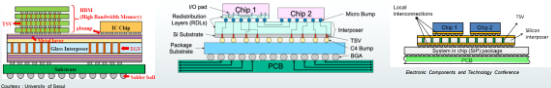


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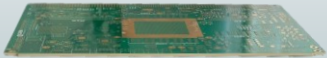
WHAT IS: ULTRA HDI, IC SUBSTRATE, SLP?

Ultra HDI vs IC Substrate Vs SLP
Hetrogeneous Integration



Courtesy: University of Sussex

PCB, IC Substrate and Chip = hetrogeneous Integration





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Ultra HDI Design Guideline

PCB design
guidelines (printed
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ULTRA HDI DESIGN GUIDELINES 2.0





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UHDI Success

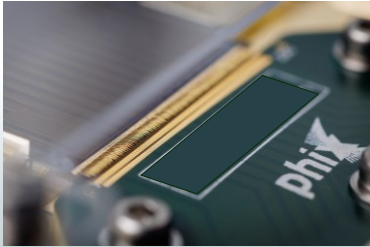
- 2 layer with extra stiffener on bottom.
- Copper 9µm + plating
- ENEPIG finish

Wire bond pads:

- 8.4mm x 6.150mm
(Min. top pad 120µm width)
- Minimum spacing 50µ
- etching tolerance: 10%

Laser holes:

- 150µm microvia pad diameter
- 50µm laser drill





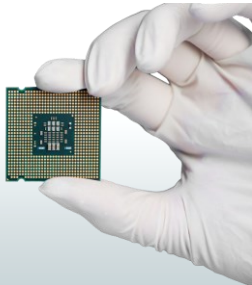
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WHAT IS THE CURRENT STATUS?

Content

1. What is Multilayer, HDI and Ultra HDI?
2. IPC standards
3. Production availability





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IPC STANDARDS

IPC Standards for HDI

IPC-2226

Sectional Design Standard for High Density Interconnect (HDI) Boards

IPC-6012

Qualification and Performance Specification for Rigid Printed Boards (replaced IPC-6016)

IPC-4104

Specification for High Density Interconnect (HDI) and Microvia Materials

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IPC STANDARDS

IPC Standards for Printed Boards and IC Substrates

Type	Design	Performance	Acceptability	Materials
Multilayer	IPC-2221/2222	IPC-6012F (13)	IPC-A-600K	IPC-4101
HDI	IPC-2221/2223	IPC-6012F (13)	IPC-A-600K	IPC-4104
UHDI	IPC-2229 (2025?)	IPC-6019 (2025?)	TBA	IPC-4101/4103++
IC Substrates	??	IPC-6921(FDIR)*	IPC-6921*	None

Printed Electronics
System in Package
Wearables
Additively Manufactured
Electronics (AME)

IPC60xx Addenda
Materials
MSPB
High Frequency
Surface Finishes

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* Combined Performance and Acceptability

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IPC STANDARDS AND ACTIVITIES

IPC Activities

> Ultra HDI Leadership Group

> Update Design standard IPC-2220 series (IPC-2229)

> Update Performance standard IPC-6010 series (IPC-6019)

> IC Substrate Standard in process: IPC-6921

Assembly
IPC-610/J-Std-001

Design
IPC-2220

Test
TM-650..

Materials

Performance
IPC-6010

UHDI

IC Substrate

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IPC STANDARDS AND ACTIVITIES

Products Beyond IPC 2226 Criteria

IC Substrate

Table S-1 Typical Values for Substrate Construction		IPC 2226 Table S-1	Existing	Ultra HDI PCB				IC Substrate	
			Level C	50-40 um		40-30 um	30-20um	< 20 um	
IPC 2226 Table S-1				Substrate Like PCB (SLP)					
Traditional subtractive PCB Processing									
ES	Plated conductor trace width	60 um (2.4 in)	40um-20um	N/A (undefined)	N/A	N/A	N/A		
FS	Plated conductor spacing	60 um (2.4 in) (1)	40um-30um	20um-40um	20um-30um	6um-20um	6um-20um		
High end PCB subtractive Processing									
S	Minimum plated conductor width	(See IPC 2226, Table S-1)	3um-8.5um	1-3 um	N/A	N/A	N/A		
S	Minimum plated conductor spacing	(See IPC 2226, Table S-1)	3um-17.3um	None	None	None	None		
Additive or semi additive processing									
A	Plated conductor trace width	(See IPC 2226, Table S-1)	3um-8.5um	1-3 um	N/A	N/A	N/A		
A	Plated conductor spacing	(See IPC 2226, Table S-1)	3um-17.3um	None	None	None	None		
IC Substrate									
A	Plated conductor trace width	(See IPC 2226, Table S-1)	3um-8.5um	1-3 um	N/A	N/A	N/A		
A	Plated conductor spacing	(See IPC 2226, Table S-1)	3um-17.3um	None	None	None	None		

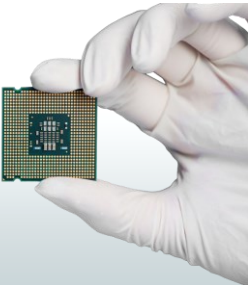
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WHAT IS THE CURRENT STATUS?

Content

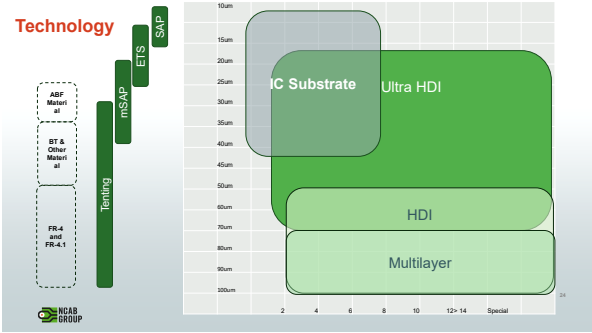
1. What is: Ultra HDI, IC Substrate, SLP?
2. IPC standards and activities
3. Production availability



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Global Availability

Type	Prototypes	HMLV	Volume	Full availability
Multilayer	All continents	All continents	ASIA	Limited Availability
HDI	All continents	All continents	ASIA/AM	Low availability
UHDI	ASIA (EU/US) (MOV)	ASIA (EU/US) (MOV)	ASIA	Capacity Limitations
IC Substrates	ASIA (EU/US) (MOV)	ASIA (EU/US) (MOV)	ASIA	



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PRODUCTION AVAILABILITY

New Technology Impact on Environment

Additive manufacturing Processes: mSAP/SAP/ETS

Energy: > 70% reduction

Etched Copper: >90% reduction

Copper consume: >90% reduction

Material consume related to design reduction and technology.

Additive manufacturing is the future!

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THANK YOU

Questions?



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