ELECTRONIC COAST EVENT

Business Unit – Electrical Solutions
Application Engineering

2024-10-31

AGENDA TITLE

01 Introduction AT&S

02 Embedding:
Capabilities + Design Rules

03 Modified Semi Additive Process (mSAP)

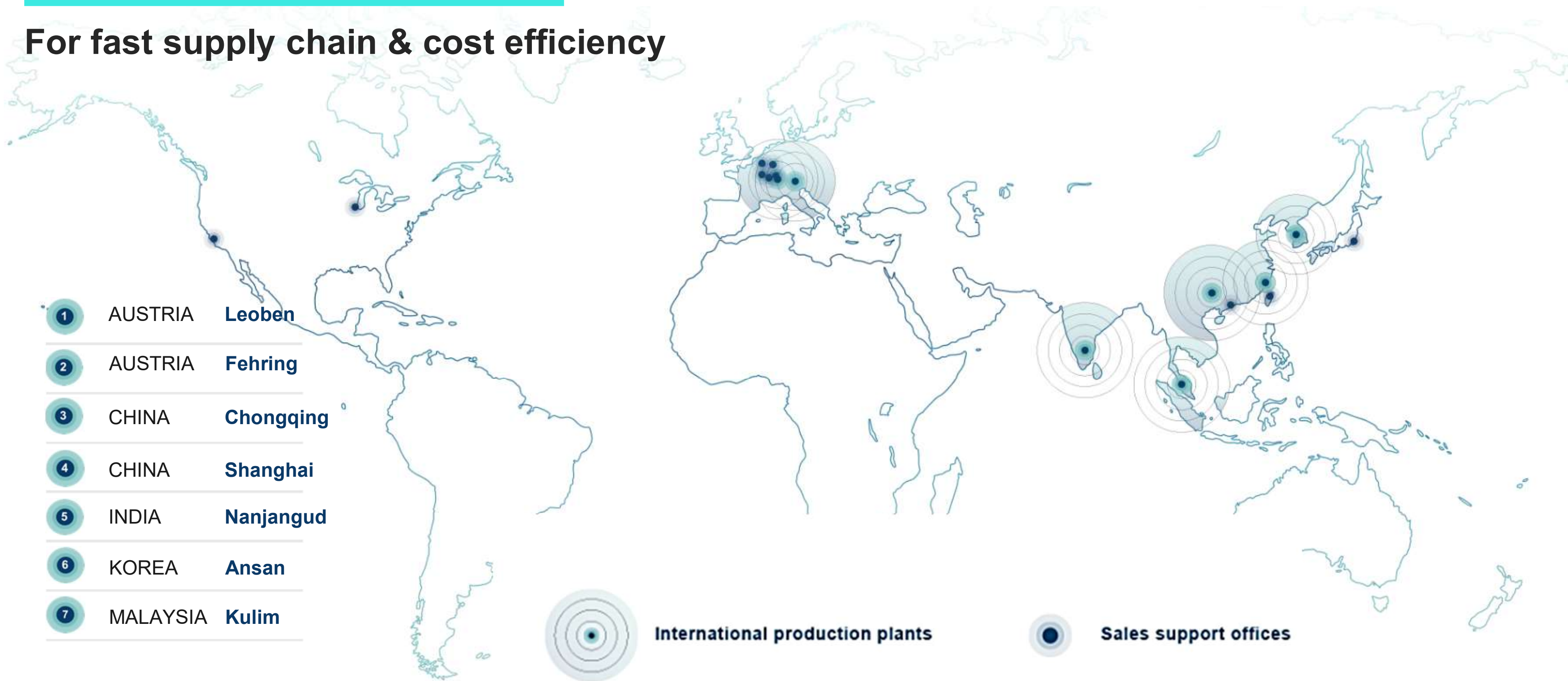
04 Substrate Like PCB (SLP)

05 2.5D Cavity + Semi Flex

06 ZiC Technology

07 Already developed & manufactured Applications

08 Plant capabilities


GLOBAL FOOTPRINT
For fast supply chain & cost efficiency
1 AUSTRIA Leoben
2 AUSTRIA Fehring
3 CHINA Chongqing
4 CHINA Shanghai
5 INDIA Nanjangud
6 KOREA Ansan
7 MALAYSIA Kulim
International production plants
Sales support offices

WORLD LEADING HIGH-TECH PCB & IC SUBSTRATES COMPANY

€ 1.55bn
revenue in FY 2023/24

#2
high-end PCB producer worldwide*

#5
IC substrates producer worldwide**

Top 10
Among the top ten PCB and IC substrates manufacturers worldwide

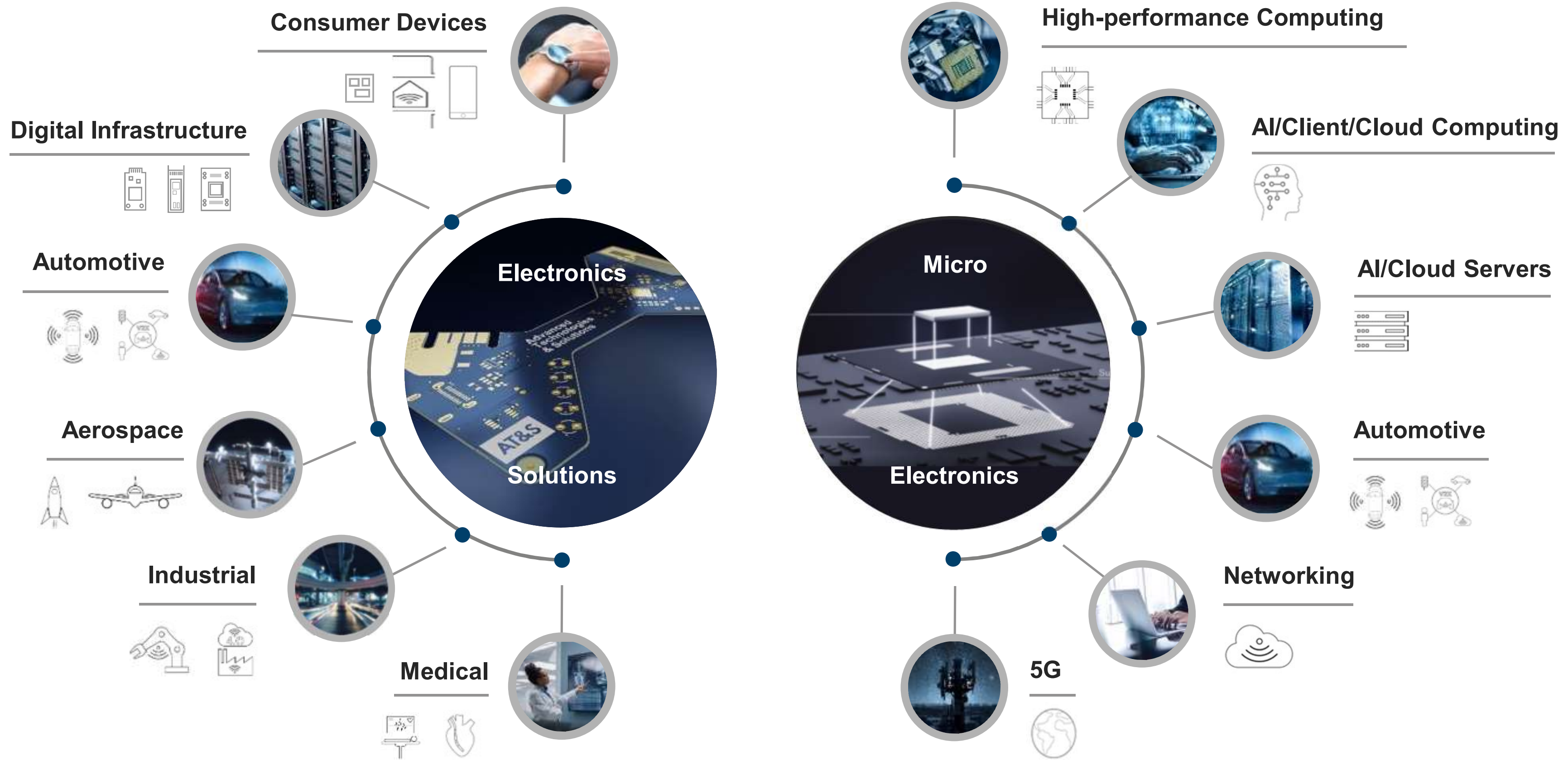
~13,500
employees

7
Locations

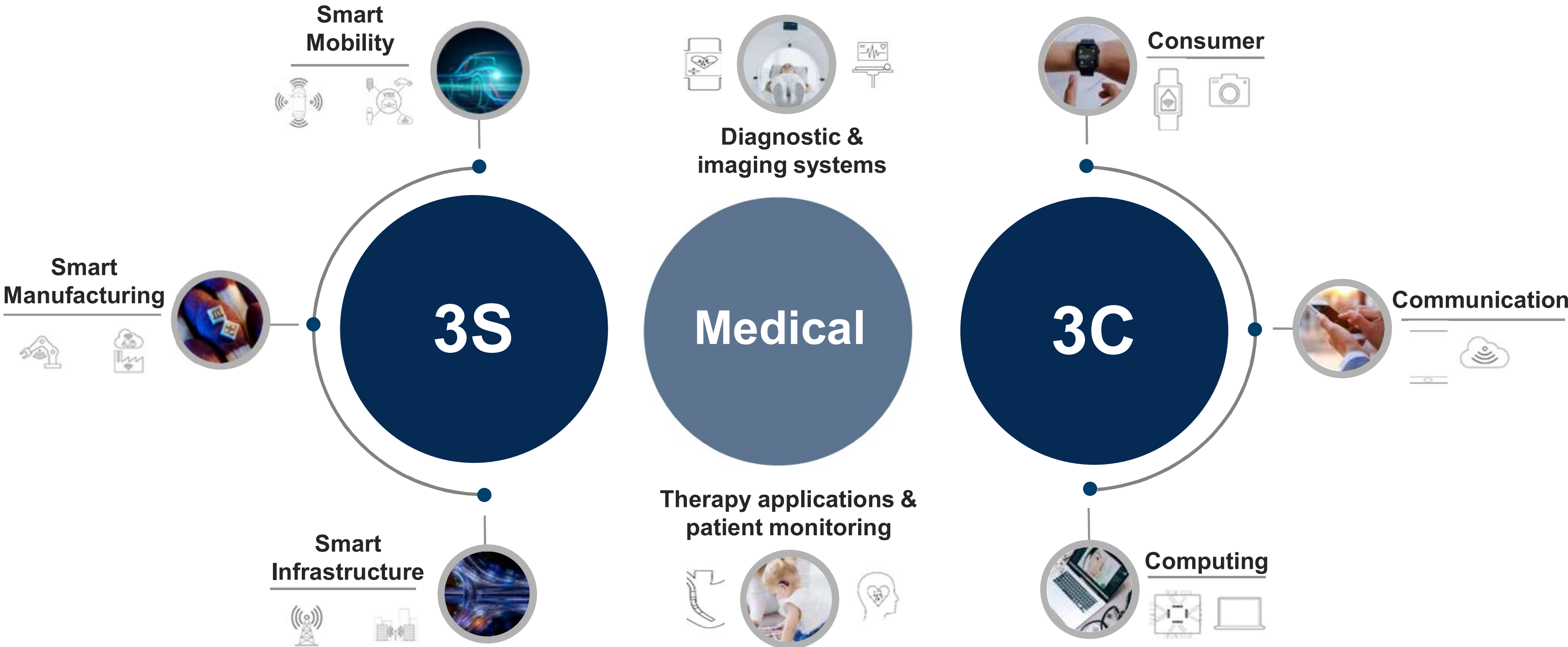
12
Plants

*Source: Prismark, CY2022, as of 15.05.2023
**Source: Prismark, CY2022, as of 31.08.2023

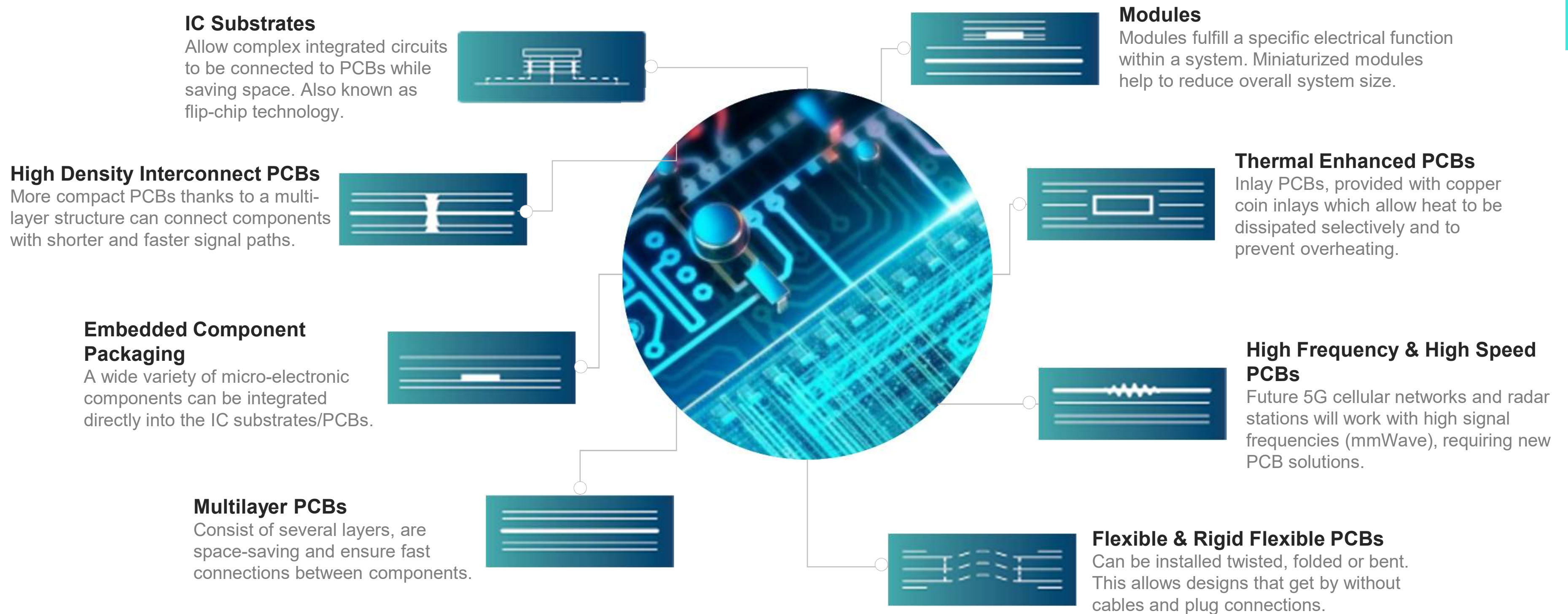
MARKET SEGMENTS & PRODUCT APPLICATIONS



BU ELECTRONICS SOLUTIONS



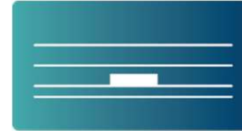
AT&S PRODUCT PORTFOLIO



AT&S SPECIAL TECHNOLOGY PORTFOLIO

mSAP Technology

Innovative production-process for radically thin PCBs used in highly compact devices



ECP® Technology

Space-saving through vertical embedding of components leads to significant form factor reduction

Z-Interconnect Technology

Z-Interconnect is AT&S's answer to the arising challenges of miniaturization, high signal speeds, high density and increasing layer count

2.5D® Technology

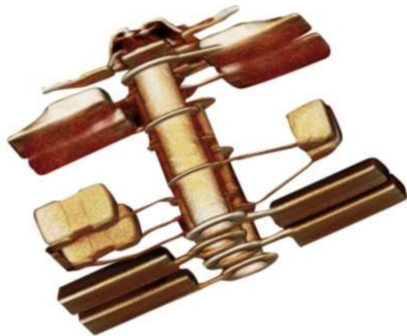
Cost-effective creation of cavities in multilayer circuit boards for miniaturized designs

WHAT IS EMBEDDING TECHNOLOGY

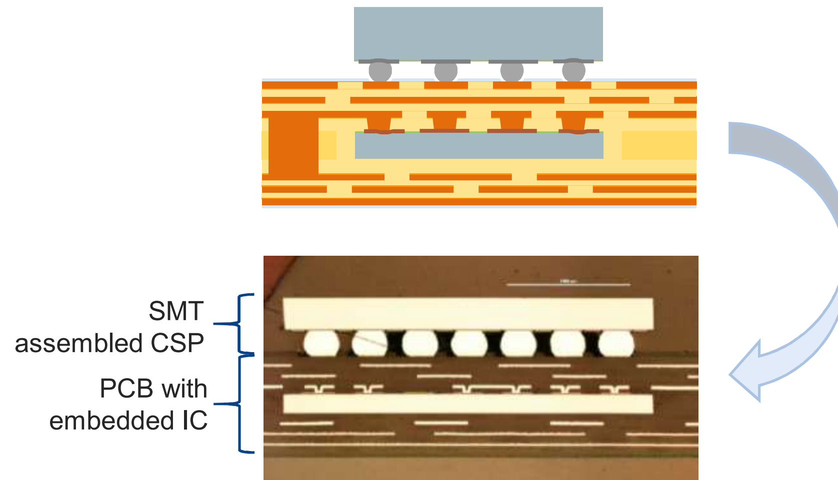
AT&S ECP® - Embedded Component Package

ECP® (Embedded Component Packaging) uses the free space in an organic, laminate substrate (Printed Circuit Board) for **active and/or passive** components

Components are integrated in the core of the PCB and connected by copper plated micro vias



CT image of embedded capacitors in a 4 layer PCB



AT&S EMB TECHNOLOGY OVERVIEW

In mass Production

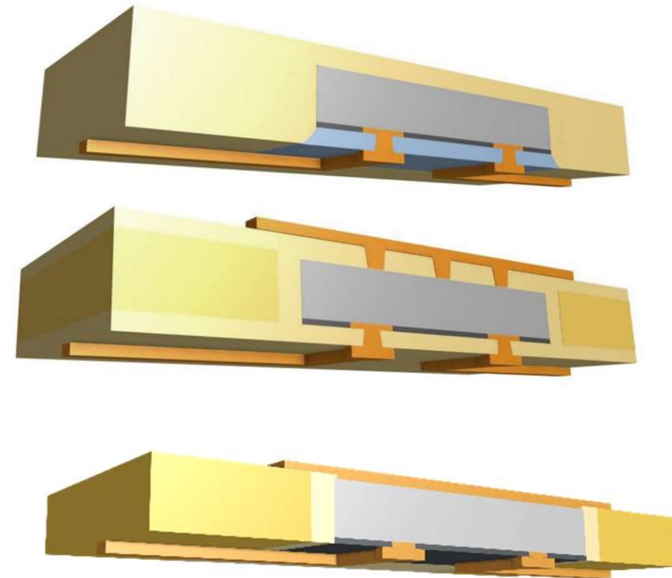
ECP®
The first choice for cost-efficient packaging of passive and small-size active components

CENTER CORE EMBEDDING
The preferred packaging technology for power applications with double-sided component connection

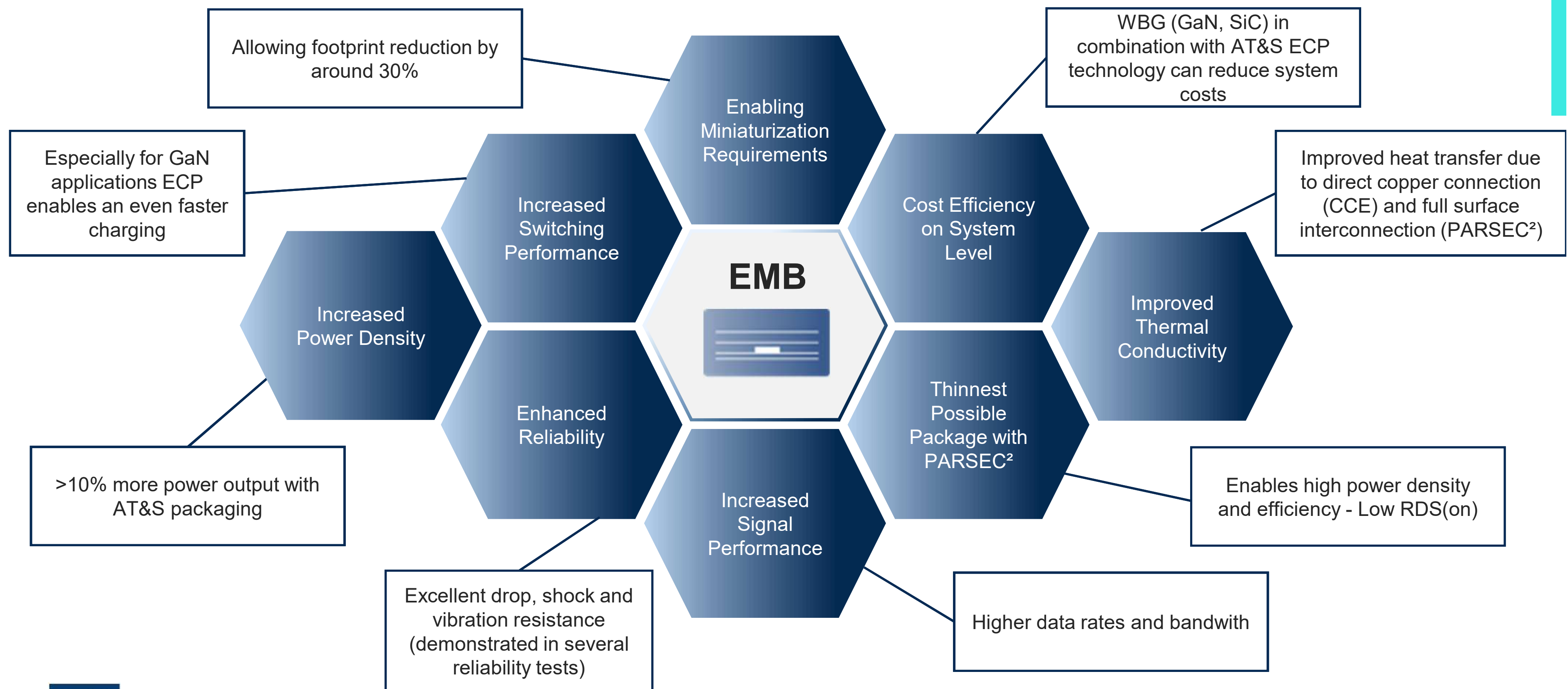
In Process Evaluation

PARSEC²
The thinnest possible embedded package for active components with a wide range of metallization types

Process Validation ongoing

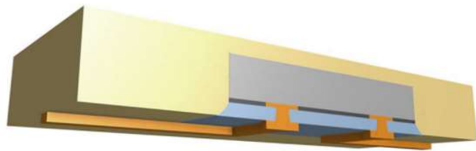


EMBEDDING TECHNOLOGY BENEFITS

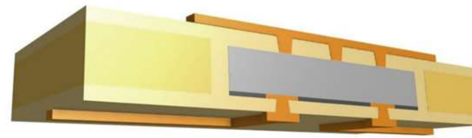


EMBEDDING OF COMPONENTS

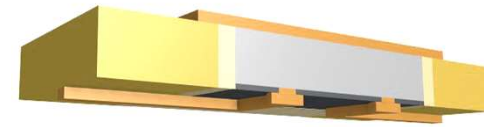
ECP®
The first choice for cost-efficient packaging of passive and small-size active components



CENTER CORE EMBEDDING
The preferred packaging technology for power applications with double-sided component connection



PARSEC²
The thinnest possible embedded package for active component with a wide range of metallization types



Integrate active and passive Components

- Bare dies
- Single / double sided connected
- Si / GaAs / GaN …
- Pad termination: Copper, Au, Al

Performance Benefits

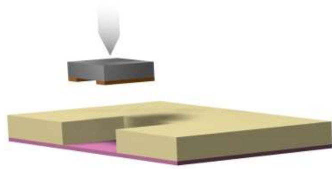
- Reduce Transmission losses
- Minimize Feeding Network length
- Split of Signal Path and Thermal Path
- More accurate Signal Path due Micro Via interconnection

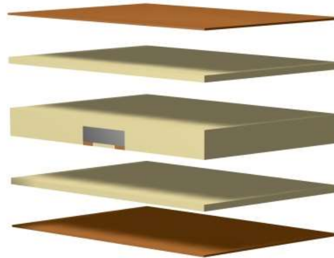
Additional Benefits

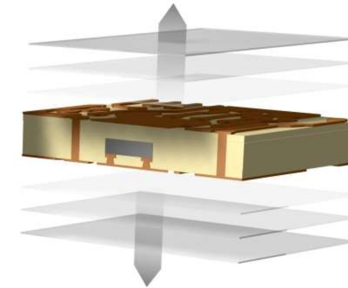
- High Reliable Performance
- Stable against vibration
- Increase Packaging density
- Reduce weight
- Reverse Engineering protection

EMBEDDING OF COMPONENTS

Center Core Embedding Process Flow







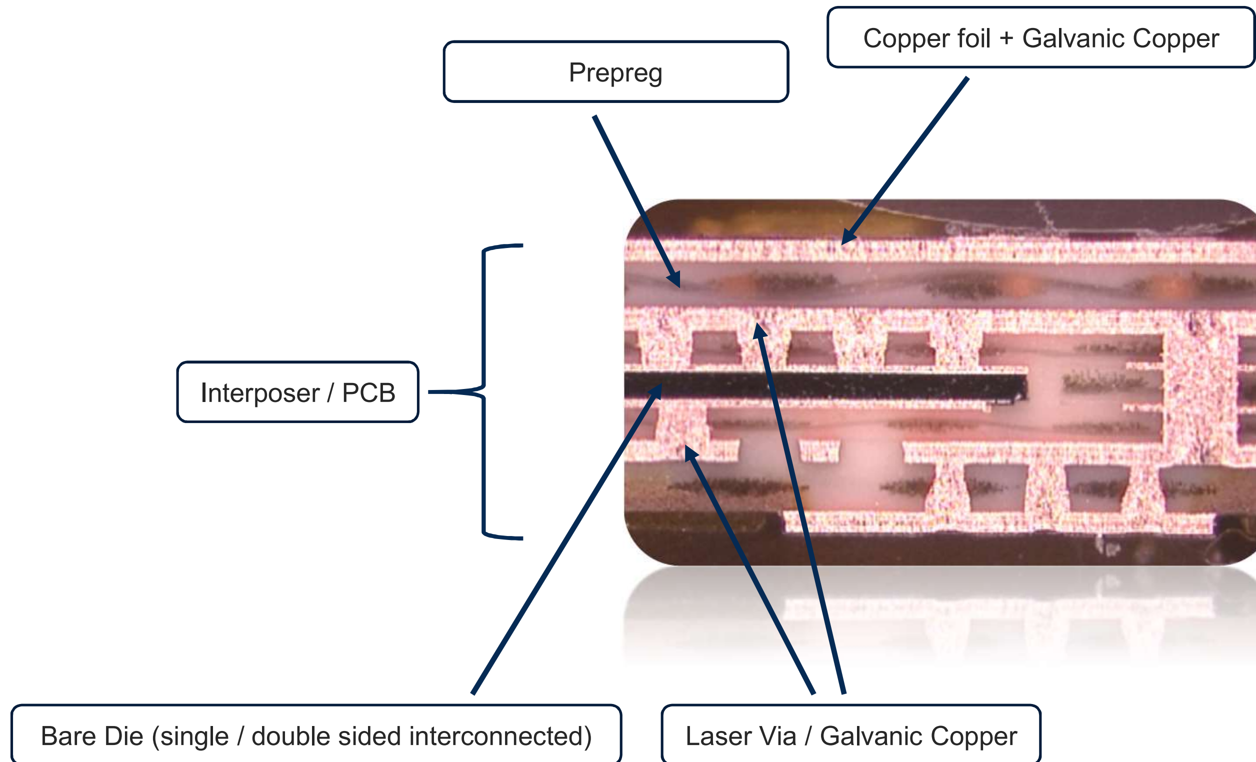
- Core preparation
- Cavity cutting
- Carrier lamination
- Component assembly (Face Down)

- Soft lamination
- Carrier removal
- Final lamination

- Laser drilling (component interconnection)
- Mechanical drilling (PTH)
- Plating and structuring
- Testing

EMBEDDING OF COMPONENTS

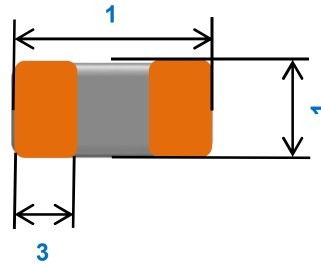
Center Core Embedding



Component Requirements

Component Parameter							
1 Min. Size [µm]	1 Max. Size [mm]	2 Min. Nominal Thickness [µm]	2 Max. Nominal Thickness [µm]	Thickness Tolerance	3 Min. Pad Diameter [µm]	Pad Surface	4 Copper Thickness [µm]
300 x 600 (0201)	8 x 8	60	300	± 10 µm*)	200 (LaserØ: 80 µm)	Copper only	Min. 5 (preferred: 7 – 10)

*) Preferred tolerances, wider tolerances have to be discussed during specific project review



Electrical Test

- **Capabilities**
  - **Open / Short (please refer to the chapter "General Capabilities & Design Rules")**
  - **Passives (Resistor & Capacitor)**
  - **Actives (Continuity – / Diode – Test)**

- **Test parameter**
  - **Passives *)**

Resistor			Capacitor		
Min.	**Max.**	**Tolerance**	**Min.**	**Max.**	**Tolerance**
1 Ω	10 MΩ	± 0,5 %	0,1 pF	100 µF	± 2 % ± 0,03 pF
10 MΩ	50 MΩ	± 2 %			

*) inductivities have to be discussed during specific project review

  - **Continuity – (Diode)Test for Actives**

A diode is defined as:
- a polar connection between two systems
- with defined voltage and current
- with plus/minus tolerances
- and with a optional voltage limitation for the test

Current		Voltage
Min.	**Max.**	**Max.**
100 µA	50 mA	10 V

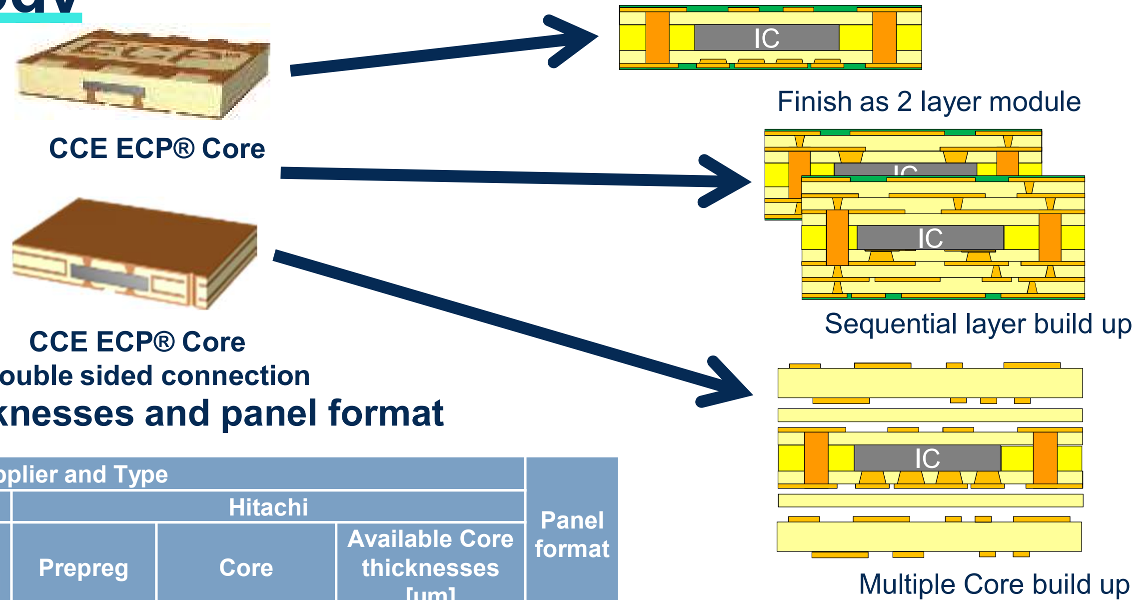
A single diode measuring consists of:
- the defined current
- the expected voltage
- the allowed tolerances and the voltage limitation which must not exceeded during the test to protect the diode.

- **Note: Functional testing not available! Capabilities for actives has to be discussed during specific project review!**

CCE ECP® - Technology

➢ Capabilities

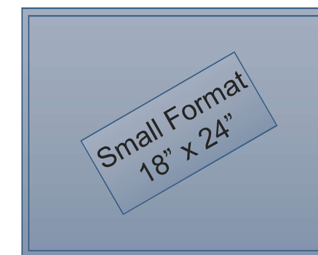
- ✓ 1 embedded Core
- ✓ Sequential build up (up to 10 layers)
- ✓ Multiple Core build up (up to 8 layers)



➢ Qualified base material, core thicknesses and panel format

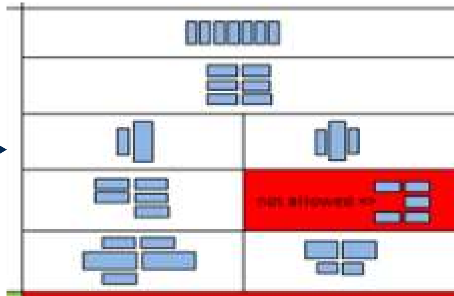
Material Properties	Supplier and Type						Panel format
	Panasonic			Hitachi			
	Prepreg	Core	Available Core thicknesses [µm]	Prepreg	Core	Available Core thicknesses [µm]	
High TG (170°, halogenreduced)	R-1570	R-1577	80, 100, 114, 130, 150, 180,200,230,280	-	-		18" x 24" only
Low CTE (180°, halogenreduced)	-	-	-	GEA-679FG(S)	MCL-E679FGB(S)	80, 110, 160, 200,250	
Low CTE (250°, halogenreduced)	-	-	-	GEA-700	MCL-E-700*)	100, 150, 260, 310	
Low CTE (270°, halogenreduced)	-	-	-	GEA-770	MCL-E-770*)	100, 150, 200, 270, 310	

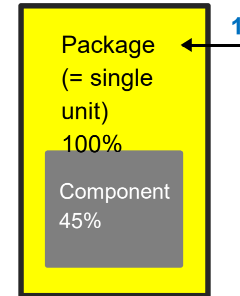
*) For Demonstrators only!

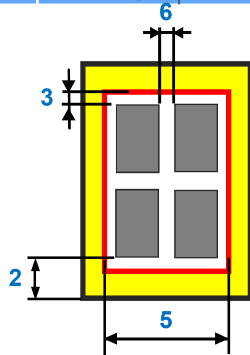


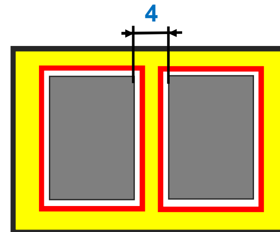
Embedded Component Scope*)

No.	Topic	Parameter
1	Maximum Ratio: Component Area / Card Area	45% [1)]
2	Distance Package Edge to Component Edge (dicing)	250µm (4 Layer board)
3	Cavity Width (Component Edge to Cavity Edge)	75µm
4	minimum distance single component to single component	350µm
	Grouped Components	Yes
5	Grouped Components: Max. cavity area	15mm²
	Grouped Components: Architecture	Symmetrical (cavity shape)
6	Grouped Components: Distance Component - Component	50µm to 100µm (preferred 75µm)









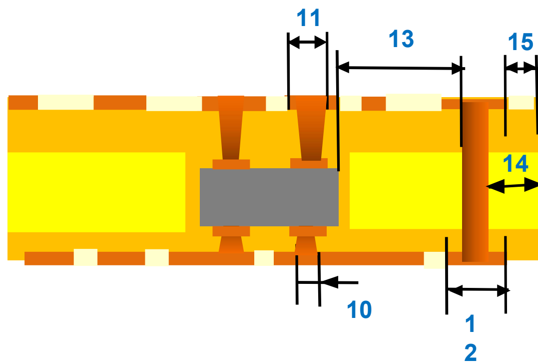
Legend	
Black line	Package outline
Red line	Cavity outline
Grey	component
Yellow	Base material
Brown	copper

1) valid for a component thickness of max. 150µm, thicker components have to evaluated separately during project phase

) For values which are not listed in this table, please refer to the chapter *"General Capabilities & Design Rules"

AT&S

Embedded Component Scope*)



8: Example (component to core ratio):

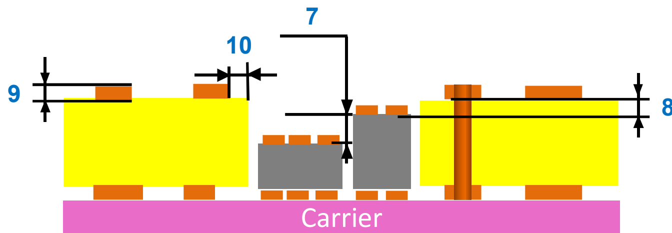
Nominal component thickness: 100µm
Tolerance: ± 10µm
Ratio Min: 1 : 1,05
Ratio Max: 1 : 1,3

Core thickness = nominal component thickness + tolerance x ratio

Core thickness min = (100µm + 10µm) x 1,05 =115,5µm

Core thickness max = (100µm + 10µm) x 1,3 = 143µm

Used core should be within 115µm and 143µm!!



No.	Topic	Parameter
7	Component to Component Thickness Variation: (Core Thickness < 200µm)	10%
	Component to Component Thickness Variation: (Core Thickness > 200µm)	5%
8	Ratio: Max. component thickness to nominal core thickness (w/o base copper)	
	Nominal Component thickness: 60µm up to 100µm	Min.: 1 : 1,05 Max.: 1 : 1,3
	Nominal Component thickness: 101µm up to 200µm	Min.: 1: 1,05 Max.: 1 : 1,15
	Nominal Component thickness: 201µm up to 300µm	Min.: 1: 1,05 Max.: 1 : 1,1
9	CU Thickness CCE Core [1)]	max 30µm (preferred 25µm)
10	Cu to cavity edge [1)]	Min. 50µm
	Laser – Diameter: Connection to Component Front	Depends on dielectric height*)
11	Laser – Diameter: Connection to Component Back	Depends on dielectric height*)
	Different Laser – Diameters	Possible, difference max. 20µm
12	Minimum Padsize for Mechanical drilled PTH	Min. DrillØ + 150µm (preferred + 200µm)
13	Distance PTH Edge to Component Edge (no copper on core)	175µm
	Distance PTH Edge to Component Edge (copper on core) [1)]	250µm
14	Distance PTH Edge to Package Edge (dicing)	170µm (4 Layer board)
15	Distance Package Edge to Copper outer layer (dicing)	Min. 50µm (4 Layer) (preferred 100µm)
	Distance Package Edge to Copper inner layer (dicing)	100µm

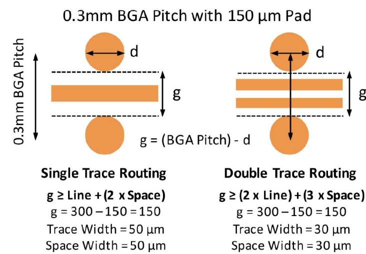
1) For demonstrators only! Preferred option → no copper on CCE ECP® Core
) For values which are not listed in this table, please refer to the chapter *"General Capabilities & Design Rules"

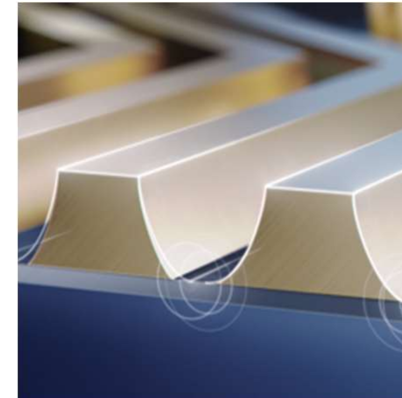
MSAP TECH OVERVIEW

Achievements with mSAP

- Increase PCB routing density for fine-pitch BGA packages (≤30µm line/spacing)
- Reduce the number of layers required for fan-out (or pressing cycles)
- Increase Component Pitch Density
- Reduce the overall PCB thickness
- Optimize signal transmission
- Higher performance at reduced mainboard sizes

Number of Traces	Required Line / Space Width
1	g ≥ Line Width + (2 x Space Width)
2	g ≥ (2 x Line Width) + (3 x Space Width)
3	g ≥ (3 x Line Width) + (5 x Space Width)



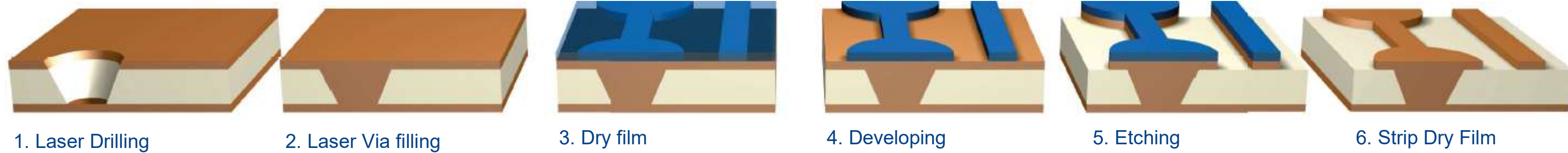

Conductor tracks standard

Conductor tracks mSAP

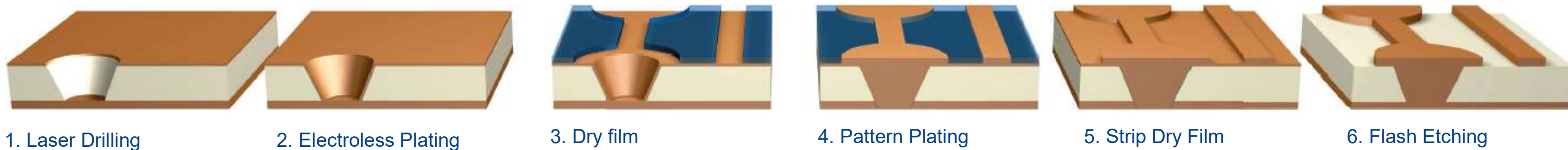
PROCESS FLOW

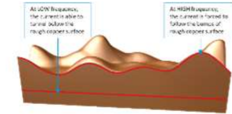
Subtractive vs. mSAP

Subtractive Process



mSAP Process



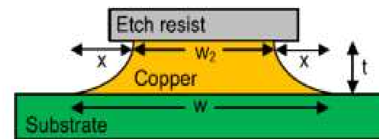


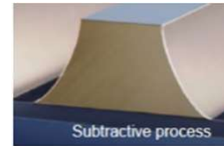
MODIFIED SEMI ADDITIVE PROCESS (MSAP)

Influence of Trace Geometry

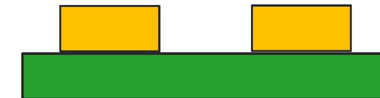
- Tighter X-section variance
  - reduced skin effect (shorter edge length)
  - better control of coupling between two copper planes
  - better control of impedance
- Tighter track width tolerance
  - improved impedance variation
- Lower line / space
  - tighter coupling between two copper planes

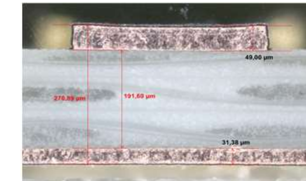
Subtractive

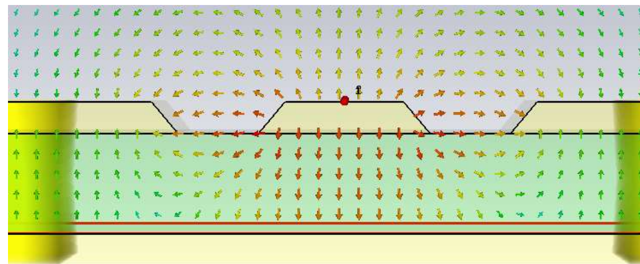


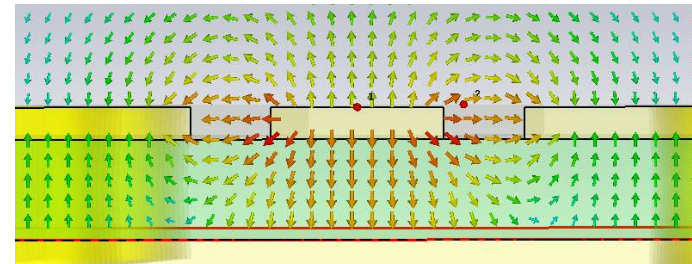


mSAP

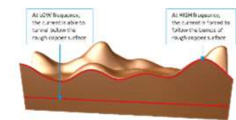








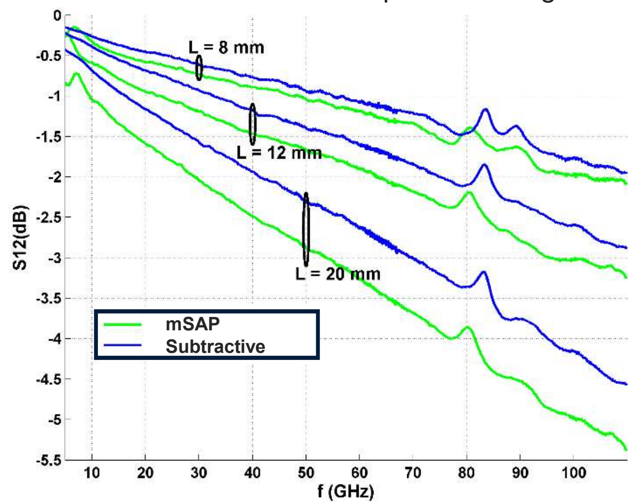
E - field distribution subtractive vs mSAP

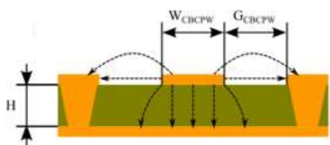


SUBTRACTIVE VS. MSAP

Impact on Signal Loss

Conductor-backed coplanar Waveguide

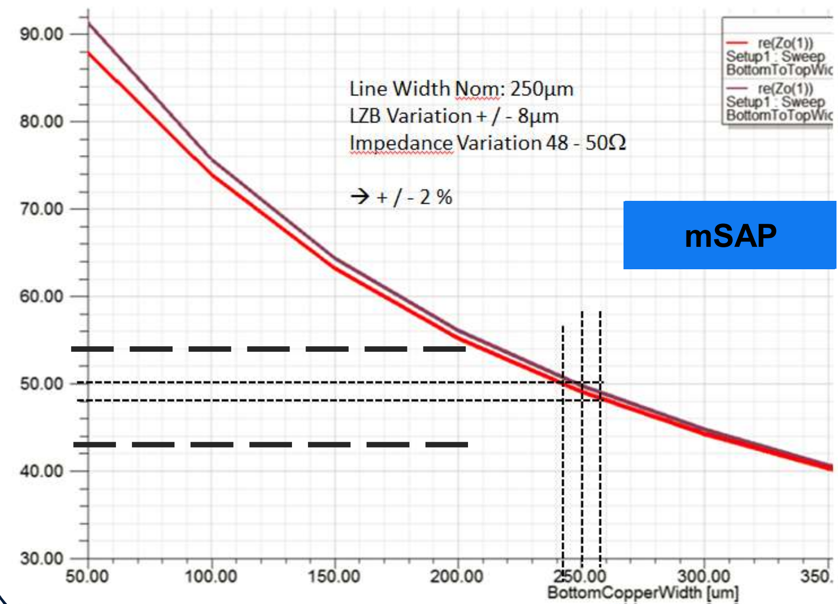




Line width mSAP: 250µm +/ 4%

Line width Panel Plating: 250µm +/- 20%

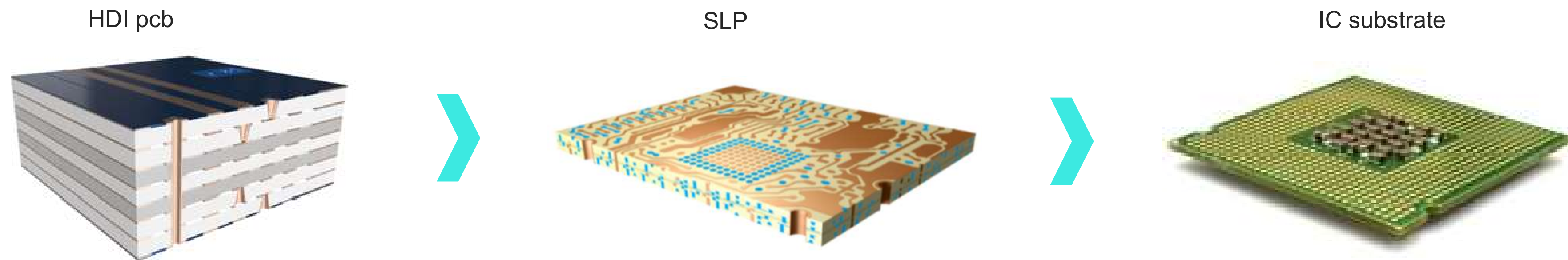
Impact on Impedance



SLP

What is a SLP?

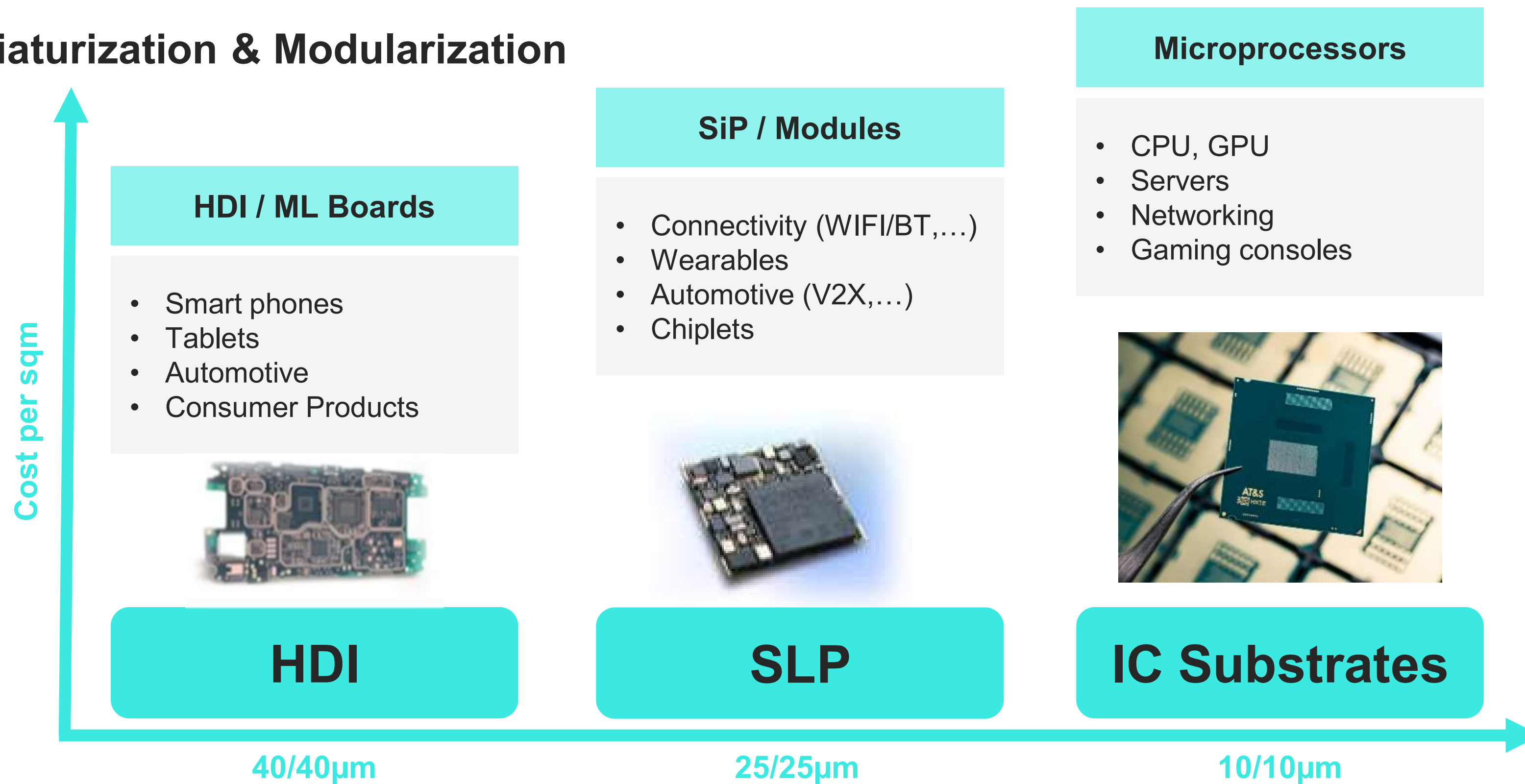
Substrate like pcb bridges the technology gap between pcb and IC substrate



A solution to achieve a higher density and a smaller form factor

SLP CONCEPT

Miniaturization & Modularization



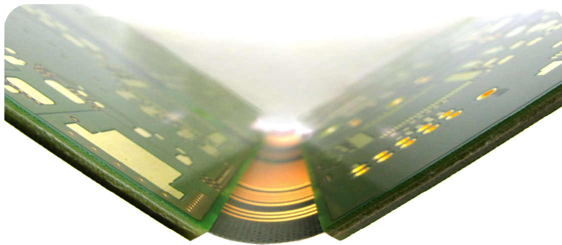
SLP @ AUSTRIA

Min. crd size	10 x 10mm
Min. PCB Thickness	0,1mm
Min. Line/Spacing	25µm/25µm (mSAP)
Thinnest PP	1017 (30-40µm)
Min. Laser Pad size/drill size	140/50µm
Min. pitch size	250µm
Material	MGC: 832NS Resonac: MCL-E-700G(R) MCL-E-705G(L) EMC: EM526
Surface Finish for SLP	ENIG ENEPIG OSP
Special	Dicing

2.5D® TECHNOLOGY PLATFORM

2.5D®

2.5D® Rigid-Flexible



Proven reliability for *Flex-to-install* applications

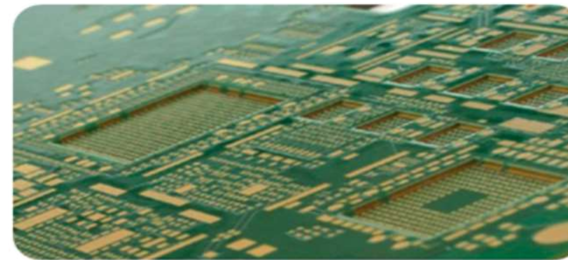
Polyimide-free materials

No mechanical damage of flexible layers

Symmetrical and thin build ups possible

HDI Design guide lines

2.5D® Cavity



Wide range of base materials (e.g. High Speed, High Tg,…)

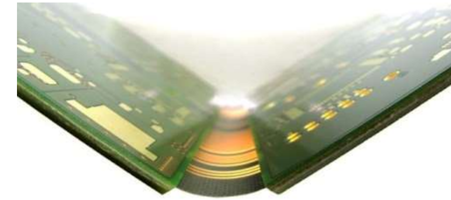
No limitations in shape and depth of cavity

Surface finishes in cavities (e.g.. ENiG, OSP,…)

Several depths can be achieved in 1 card

Solder mask in cavity

2.5D® SEMI-FLEXIBLE



- Usage of epoxy-based materials → Cost advantage
- Polyimide-free → Same assembly process as rigid PCBs
- No mechanical machining (e.g. depth routing) of flexible layers
  - → Thin Build-up layers can be used
  - → Tighter thickness tolerances of flexible layers
  - → Increased Bending Performance
  - → Variable bending length possible

2.5D® semi-flexible

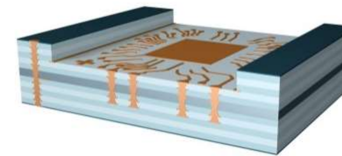
Depth routed flex

- Symmetrical build up with 1 or 2 flexible layers → Very thin Stack-ups possible
- HDI design rules remain the same (also in flex BU-layers, but not in the bend areas)

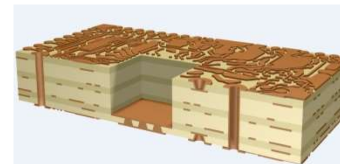
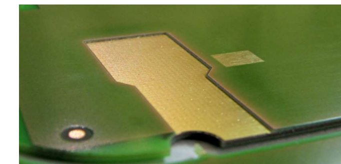
2.5D® CAVITY FORMATION

Reasons for cavities

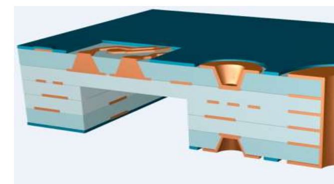
- Reduce the overall thickness of an assembled device by recessing “thick” components



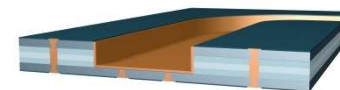
- Improve thermal management by reducing Thermal Resistance

- Improve radio performance by removing PCB material below antennas

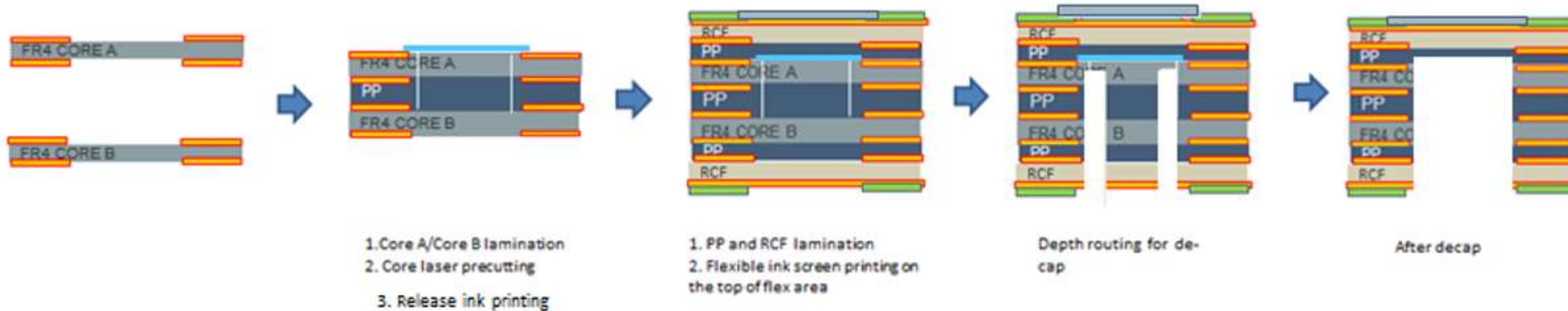


- Shielding by using metal plated cavity walls



2.5DR® SEMI-FLEX PROCESS FLOW

Semi-flex Technology with Damage Free Cap Removal – Process Flow

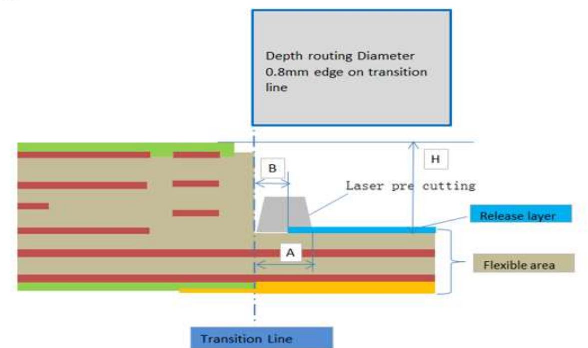


DAMAGE FREE CAP REMOVAL PROCESS

AT&S Shanghai has developed a new technical solution on cap removal method

The technology is combining laser pre-cutting and high accuracy depth control process with release layer technology.

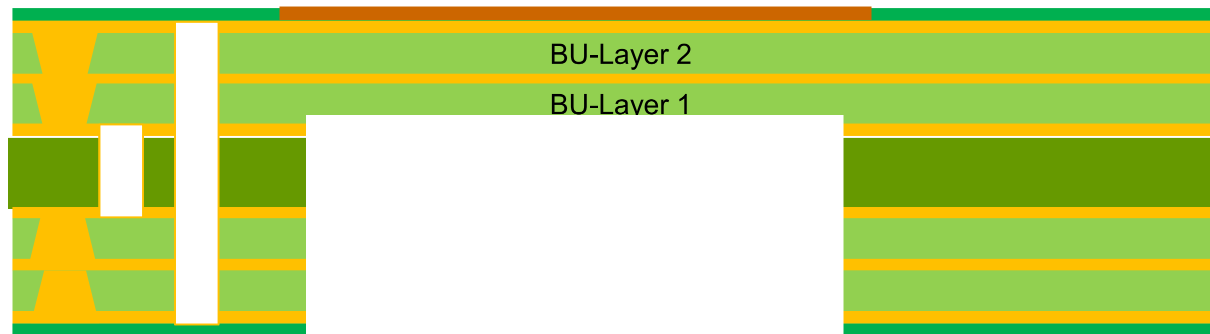
- **Decap stackup design rules**



Laser cutting diameter	A	280um
Laser hole pitch		70um
Release layer to transition line	B	150um
Depth routing diameter		0. 8mm
Depth routing tolerance (Nominal)	H	+/-75um

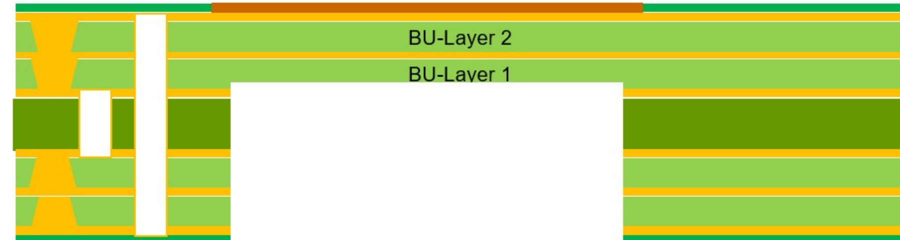
Reliable cap removal process without damage the flex region on Semi-flex PCB

2.5D® RIGID-FLEXIBLE



Design Guidline For 2.5DR (HTB)	Value	Comment
Multi-layer	>=2 Layers	
Bending area	*To be discussed with AT&S Engineering team*	*AT&S offers mechanical design support (→ p. 5)*
	1 Layer or 2 Layers	1 Layer bending: PP only
BU-Layer 1	PP: Glass cloth 1037, 0106, 1078, 1080	
BU-Layer 2	PP: Glass cloth 1037, 0106, 1078, 1080 or RCC-foil	PP is default, RCC-foil only by customer request
Cu layer(s)	</=55µm	No cross hatched design in flexible area
Assembly	Bending jig is highly recomended for assembly	AT&S offers mechanical design support (→p. 5)

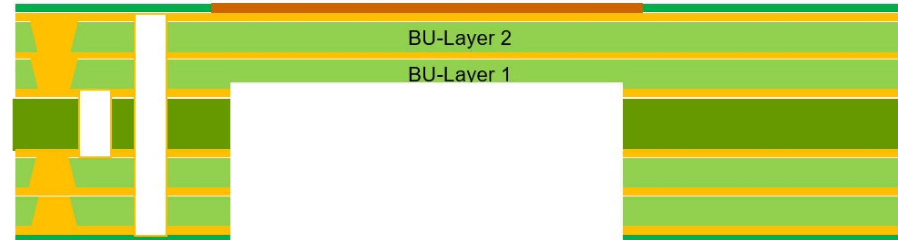
2.5D® RIGID-FLEXIBLE



2. General Design rules

Design Guideline for Shanghai 2.5DR Technology			
Category	**Design item**	**Shanghai Guideline**	**Remark**
General	2.5DR technology	Only for flex on out layer design*	Centeral core 2.5DR will be not allowed except the current CNL009000（CNL009X）, CNL601000（CNL602X）, CNL906000(CNL906X)
		Bending direction	One direction from out layer(Figure 1)
		Max. Bending times	5 times
	Surface finishing	OSP	Will update for other surface: Tin / ENIG /SIT
	Flexible area in one card	Max. 2	
	Flexible bending width	Min. 7mm(Bending <=90degree)	
		Min. 10mm(Bending 90~180degree)	
	Flexible Ink design	No SM opening allowed	
	Flexible area structure	PP, PP+PP or RCF+PP *	1. Glass fiber priority : 1037 -->1060-->1080 2. PP+PP is the default bending material, RCF + PP can be used only when customer required 3. RCF only can be on the most outer layer
Material	Flex layer count	1 layers / 2 layers	
	Flexible Base Material	Panasonic 1551WN /Shengyi S1000B/Doosan DSF-400G	TFC required for other type of PP
	Rigid SM ink	Sun chemical CAWN2619	TFC required for other type of SM ink
	Flexible ink	Tamura PAF-300-8A	
	ID ink on Flex ink area	TFC required for ID on flex ink area	

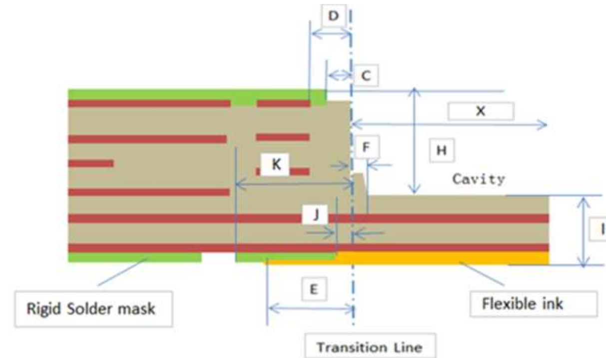
2.5D® RIGID-FLEXIBLE



Design item	AT&S NAN Guideline	Remark
Bending	Bending direction	One direction from outer layer (Customer shall specify the bending direction in the data package)
	Max. Bending times	Depending upon copper thickness, dielectric thickness, type of prepreg and copper distribution. But simulation to be done for the confirmation
Layer count	>/= 2 Layers	
Flexible layers	1 layer or 2 layer	Capable with prepreg only
Cu thickness on flexible layers	<50µm	Flexible area in inner layers shall be with less Cu density (<50%) Flexible area in outer layers shall be with high Cu density (>80%)
Surface finishing	ENIG, Immersion Tin & OSP	
Flexible bending width	Min. 3mm (Bending <45degree)	
	Min. 12mm (Bending 45~180degree)	
Flexible Ink design	No SM opening allowed	Complete flexible area shall be covered with flexible SM ink
Flexible area structure BU-Layer 1 and BU-Layer 2	PP, PP+PP (Single or Max 2 Prepregs)	0106 or 1080 best suitable Prepreg type. 2116 prepreg ok with limited bending performance
Rigid SM ink	Sun chemical ink	
Flexible ink	Tamura PAF-300-8A	

2.5D® RIGID-FLEXIBLE

Design Guideline



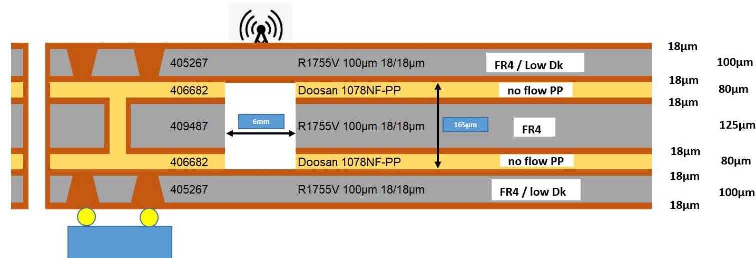
Item	Description	HTB [µm]	SHA [µm]	NAN [um]
C	Minimum Spacing between Solder Mask and cavity edge (outside cavity)	150	0	150
D	Minimum Copper edge (all layers) to cavity edge	200	200	200
E	Flexible Solder Mask overlap on rigid Solder Mask	300	300	400
H	Minimum cavity depth (include Solder Mask)	Depends on layer construction	450	450
	Maximum cavity depth (include Solder Mask)	Depends on layer construction	No Limit	No Limit
I	Minimum tolerance (include flexible ink)	+/- 50	+/- 50	+/- 50
J	Rigid Solder Mask covering far away from transition line	75	50	150
K	Solder Mask opening in the rigid part to transition line	400	400	500
X	Tolerance for Flexible width	+/- 150	+/- 150	+/- 150
F	Maximum resin flow / Offset laser cut to depth routing	400	400	400

Remark: 1) No drilling (NPTH, PTH, Laser via) allowed in semi-flexible area
2) For drilling design on rigid area follow the Copper to transition line (D)

MMWAVE ANTENNA CONCEPT

■ Air cavity backed antenna vs. Standard

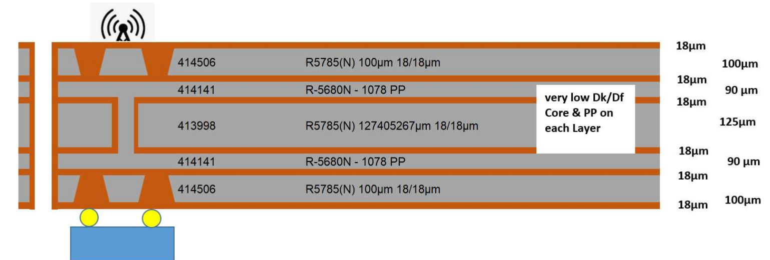
Air cavity backed



Low Cost Cacity Antenna (LCC)
Material: 1755 V or similar
Dk / Df = 4,6/ 0,013
Filled / Stacked MV, PTH
No flow PP
Cavity in FR4 and No flow PP: milling
Cavity lenght / Panel: 500mm
Cavity width: 600µm

- *Performance benefits@ 28GHz with 165µm Cavity depth*
- Directivity 16 antenna elements: +20% (22 vs. 18)
- Gain: + 130% (15dB vs. 11dB)
- Radiation efficiency: + 10% (95 vs. 85)
- **EIRP:** 3-4 dB improvement (100% better)
- **SNR:** Tx / Rx approx 6-8dB improvement (400% better)

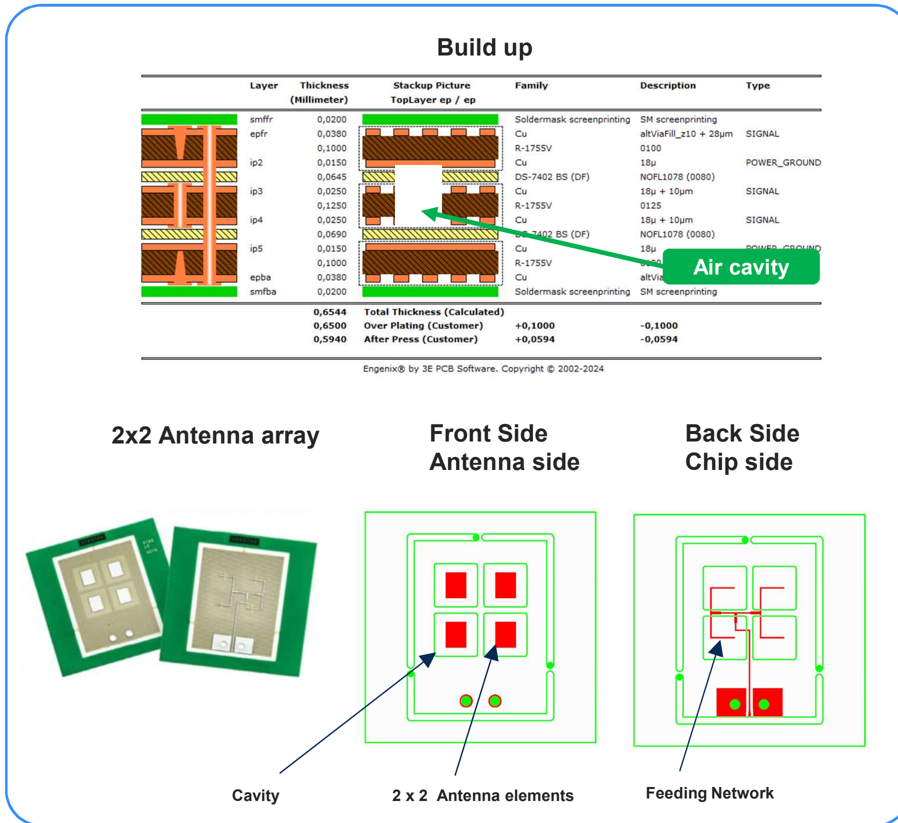
SotA



State of the art Antenna (SotA)
Material: Megtron 7
Dk / Df = 3,3 / 0,002
HVLP Cu Folie
Filled MV

MMWAVE ANTENNA CONCEPT

Air cavity backed antenna



Layer	Thickness (Millimeter)	Stackup Picture TopLayer ep / ep	Family	Description	Type
smffr	0,0200		Soldermask screenprinting	SM screenprinting	
epfr	0,0380		Cu	altViaFill_z10 + 28µm	SIGNAL
	0,1000		R-1755V	0100	
ip2	0,0150		Cu	18µ	POWER_GROUND
	0,0645		DS-7402 BS (DF)	NOFL1078 (0080)	
ip3	0,0250		Cu	18µ + 10µm	SIGNAL
	0,1250		R-1755V	0125	
ip4	0,0250		Cu	18µ + 10µm	SIGNAL
	0,0690		[illegible]-7402 BS (DF)	NOFL1078 (0080)	
ip5	0,0150		Cu	18µ	[illegible]
	0,1000		R-1755V	[illegible]	
epba	0,0380		Cu	altVia[illegible]	
smfba	0,0200		Soldermask screenprinting	SM screenprinting	
	0,6544	Total Thickness (Calculated)			
	0,6500	Over Plating (Customer)	+0,1000	-0,1000	
	0,5940	After Press (Customer)	+0,0594	-0,0594	

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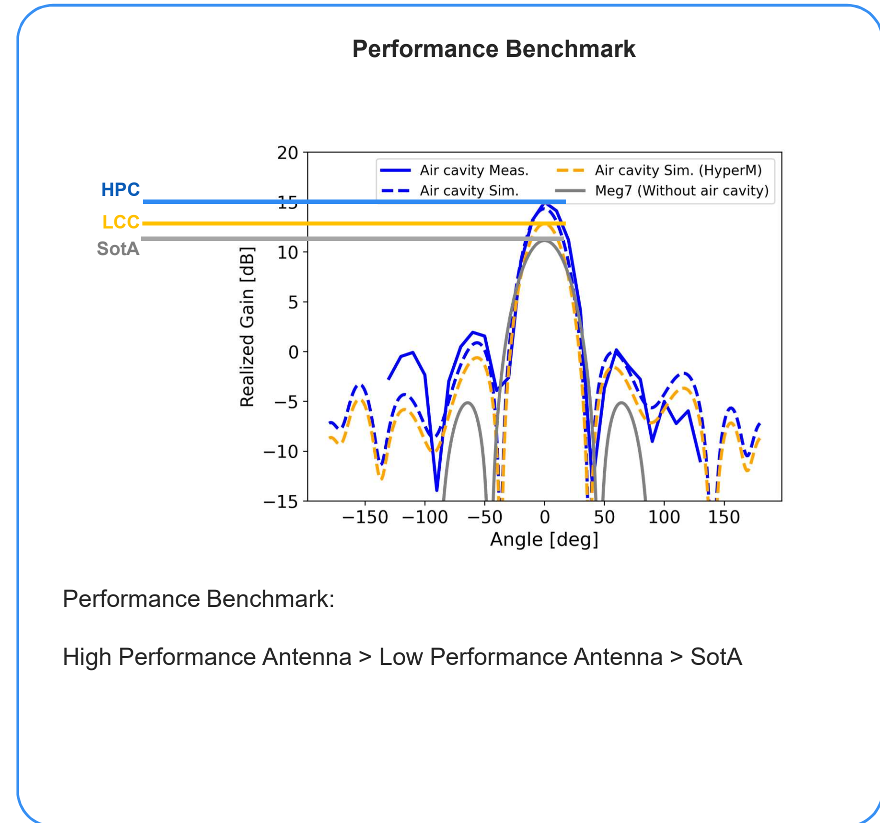
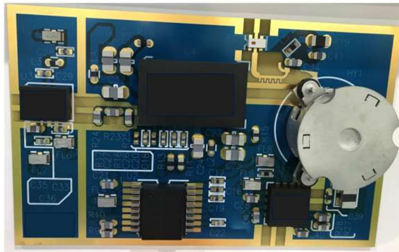


Performance Benchmark:

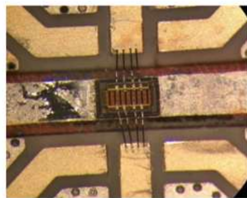
High Performance Antenna > Low Performance Antenna > SotA

CCE EMBEDDING APPLIED ON POWER AMPLIFIER RFFE MODULE FOR 5G RADIOS

State of the Art

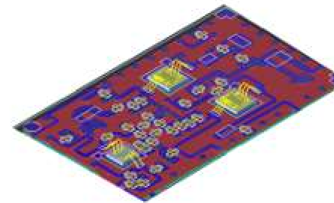


Example of 6GHz PA module with packaged GaN device size 80x40mm

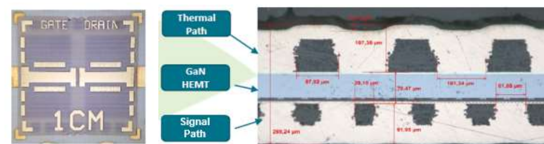


Wirebonded GaN-Si P19 device

Advanced Solution



6GHz PA module with embedded GaN device size 16x10mm



embedded GaN device

Customer Segments:

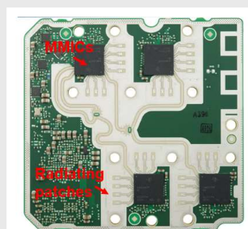
Power Amplifier for 5G Radios
5G Sub 6GHz / 5G mmWave mMIMO modules
5G indoor FWA (fixed wireless Acess)
5G outdoor FWA

Advandages of embedded Solution:

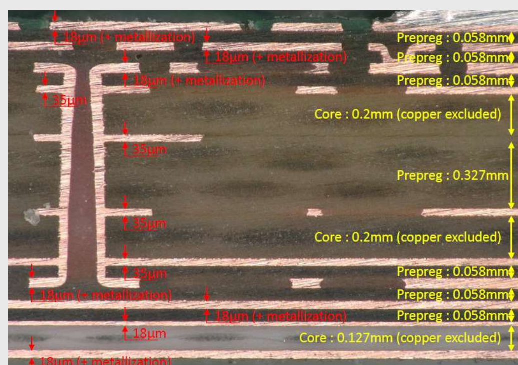
20x Footprint reduction
30% better Bandwitdth
10% better module Efficiency
10% better module Gain
10% better average Pout
15% reduced thermal Resistance
Halogenfree Base Material

Radar Sensor - 77 GHz Demonstrator

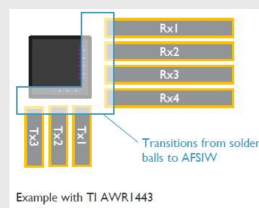
EXISTING SOLUTION



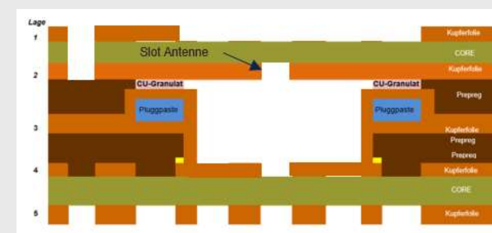
*TI transceiver (MMIC - Tx, Rx function)



PAIN POINT



AT&S DEVELOPMENT



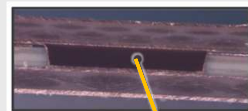
Spec	ASFIW	Tolerance	Insertion Losses	Slot Antenna	Bandwith	Directivity Radiation
Cavity depth	500µm	?	High Loss		High	
	1200µm	?	Low Loss		Low	
Width @77Ghz	3.1mm	+/-100µm				
Slot Width				100µm	high	low
				300µm	low	high
Slot Length				2200µm		
Slot Tolerance (Ws / Ls)				<50µm		
Accuracy Tolerance (Sy /Sx)				<50µm		

- All in one Solution (Mainboard, Feeding Line, Antenna
- Using existing chipset (SMD Assembly)
- Megtron 2 Material (instead of RO3003)

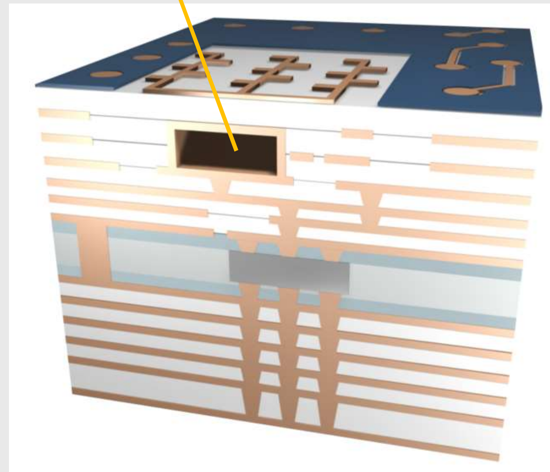
Radar Sensor - 140 GHz Demonstrator

PRODUCT FEATURES

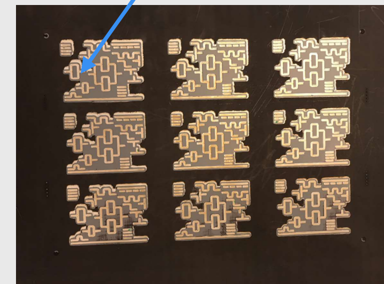
- 4 x 4 MIMO with Antenna on Chip & Antenna Array on PCB / Substrate
- Embedded CMOS Chip @ 140 GHz
- Al terminated Pads on Chip
- mmWave Antenna with high gain / high bandwidth
- AFWG as Low Loss Feeding Line
- Signal Path beyond the Chip
- Heat spreading underneath Chip
- Megtron 7 Material



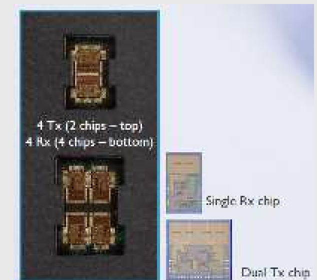
AT&S IP filed



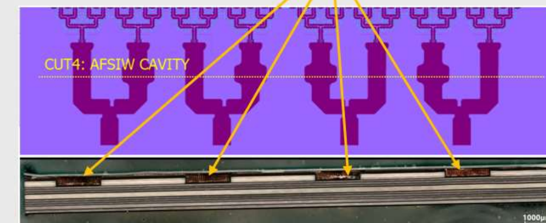
Air filled Waveguide



Antenna on Chip



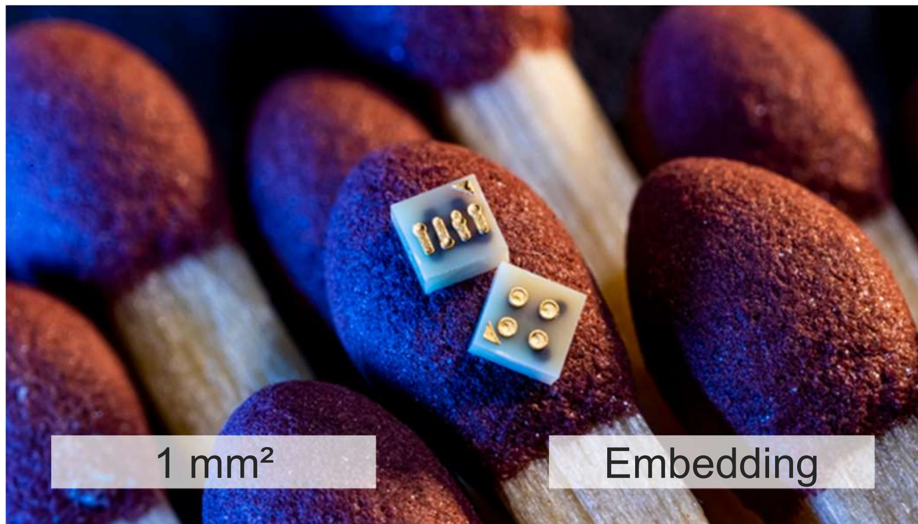
Air filled Waveguide Design vs. Cross Section

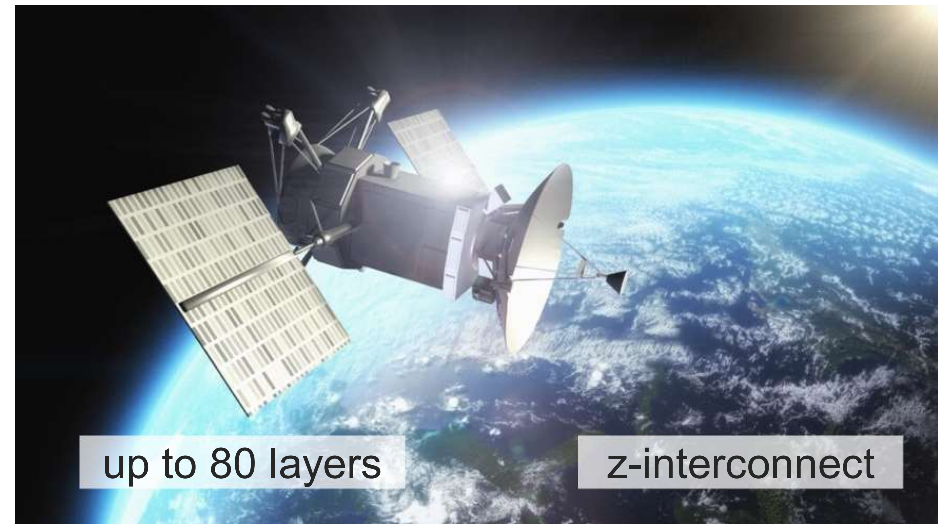


BROAD PORTFOLIO

From matchstick to satellite size

from the smallest digicam in the world	to enabling satellite technology





*Source: Prismark, CY2022, as of 15.05.2023
**Source: Prismark, CY2022, as of 15.05.2023

AT&S HINTERBERG

Headquarters - The PCB manufacturing site for high-mix, small and medium volume products with excellent R&D capabilities.

Technologies

- HDI up to 6-N-6
- Anylayer up to 14 layers
- Standard Multilayers up to 26 layers
- Substrate-Like PCB (SLP), L/S: 35µm
- High speed and high frequency boards
- Cavity in PCB with 2.5D® technology
- Embedded Component Packaging (ECP®)

1700~
Employees

40+
Years experience

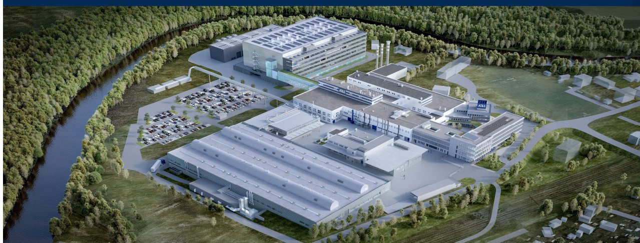
High-end
Technology focus

High
Product mix

AT&S HINTERBERG

Certifications

- EN 9100:2018
- EN ISO 50001:2018
- DS/EN ISO 13485:2016
- IATF 16949:2016
- ISO 9001:2015
- ISO 14001:2015
- ISO 45001:2018
- ISO/IEC 27001:2017
- NADCAP Accreditation
- AEO Certificate
- Sony Green Partner Certificate
- UL Listing
- IPC-QL-653



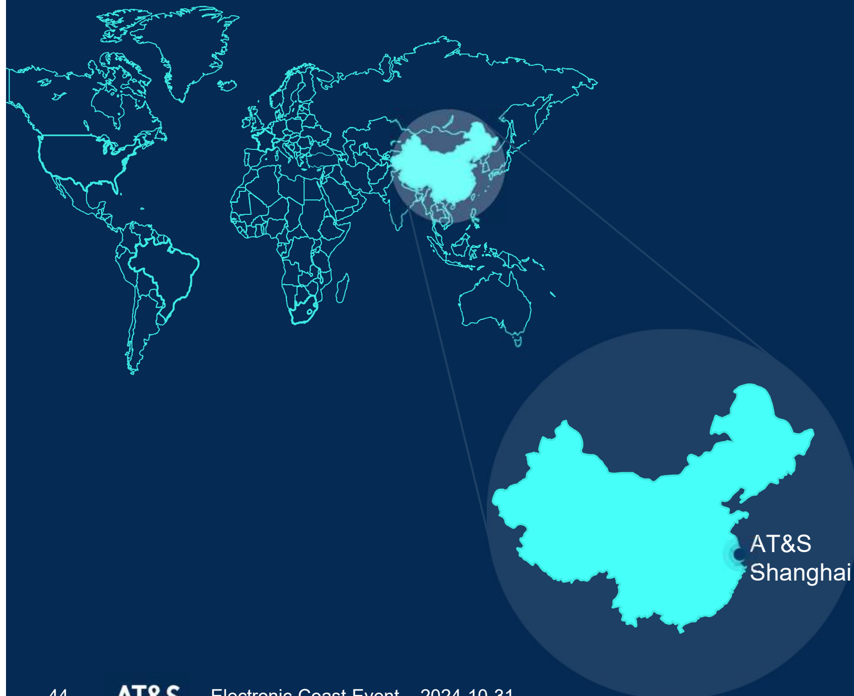
CAPABILITIES OVERVIEW*

Build-up	HDI up to 6-N-6 Anylayer up to 14 layers
Technology	ECP® - Embedded Component Packaging 2.5D® - Cavity in PCB mSAP HDI Multilayer Standard multilayer
PCB thickness	0.25mm - 3,2mm
Layer count	2 Layer - 26 Layer
Minimum line / spacing	50µm / 50µm; 20µm Copper 35µm / 35µm; 15µm Copper, mSAP
Smallest mechanical drill size	100µm
Smallest laser drill size	60µm
Solder mask	Green / Blue / Black / Red / White
Surface finish	ENIG OSP Immersion Tin ENEPIG Galvanic Nickel Hard Gold Immersion Silver HASL lead-free Carbon
Production format	18 x 24 Inch 21 x 24 Inch
Base material	FR4 from mid to high TG Halogen free materials RCF / Polyimide and PTFE Low CTE & low loss materials

Special technology and requirements on request … *

AT&S SHANGHAI

The automotive and mobile PCB manufacturing site where high-end PCB technologies come to life.



Technologies

- HDI up to 6-n-6
- Anylayer up to 16 layers
- Substrate-Like PCB (SLP), L/S: 30µm
- High speed and high frequency boards
- Cavity in PCB with 2.5D® technology
- Embedded Component Packaging (ECP®)

3900~
Employees

20+
Years experience

High-end
Technology focus

Automotive
HVM qualified

AT&S SHANGHAI

Certifications

ANSI ESD S20.20	QC080000:2017
IATF 16949:2016	Sony Green Partner
ISO 9001:2015	UL Listing
ISO 14001:2015	
ISO 45001:2018	
ISO/IEC 27001:2013	

CAPABILITIES OVERVIEW*

Build-up	HDI up to 6-N-6 Anylayer up to 16 layers
Technology	ECP® - Embedded Component Packaging 2.5D® - Cavity in PCB mSAP
PCB thickness	0.3mm - 1.6mm
Layer count	4 Layer - 16 Layer
Minimum line / spacing	40µm / 40µm; <15µm Copper 30µm / 30µm; 15µm Copper, mSAP
Smallest mechanical drill size	150µm
Smallest laser drill size	60µm
Solder mask	Green / Blue / Black Red - for samples only
Surface finish	ENIG OSP Immersion Tin ENEPIG Galvanic Nickel Hard Gold Immersion Silver
Production format	18 x 24 Inch 20 x 24 Inch 21 x 24 Inch 21.3 x 24.25 Inch for mSAP
Base material	FR4 from mid to high TG Halogen reduced materials Low Df / Dk materials Low CTE materials

Special technology and requirements on request … *

AT&S FEHRING

From simple double-sided PCBs to highly complex flexible and high-frequency PCBs - Fehring supports them.

Technologies

- Standard 2 layer PTH
- Standard multilayer (4 - 16 Layers)
- High-Frequency PCBs
- Flexible and Semi-flexible PCBs
- Rigid-flex PCBs up to 6 layers
- HDI PCBs up to 1-N-1

400~

Employees

45+

Years experience

Flexible PCB

Technology focus

AT&S FEHRING

Certifications

- ISO 9001:2015
- IATF 16949:2016
- ISO 14001:2015
- EN ISO 50001:2018
- EN 9100:2018
- DS/EN ISO 13485:2016
- ISO/IEC 27001:2017
- ISO 45001:2018
- AEO Certificate
- Sony Green Partner Certificate
- UL Listing

CAPABILITIES OVERVIEW*

Build-up	Standard PCBs up to 16 layers HDI 1-N-1
Technology	Standard 2 layer PTH Standard multilayer (4 - 16 layers) High-Frequency PCBs Flexible and Semi-flexible PCBs Rigid-flex PCBs (2 - 6 layers)
PCB thickness	0.1mm - 2.4mm
Layer count	2 Layer - 16 Layer
Minimum line / spacing	80µm / 100µm; 18µm Copper
Smallest mechanical drill size	200µm
Solder mask	Rigid: Green / Blue / Black / Red / White / Matte White Flex: Yellow
Surface finish	ENIG ENEPIG Galvanic Nickel Hard Gold HASL lead-free Immersion Tin Immersion Silver OSP Carbon
Production format	18 x 24 Inch 21 x 24 Inch
Base material	FR4 from mid to high TG Teflon (High Frequency material) Polyimide

Special technology and requirements on request … *

AT&S NANJANGUD

The state-of-the-art manufacturing facility in Nanjangud supports global electronics trends in the medical, automotive and industrial sectors with its high-end capabilities.

Technologies

- Standard multilayer PCBs (4 - 18 Layers)
- Double-sided PCBs with reinforcement
- HDI PCBs up to 4-N-4
- High frequency PCBs
- Cavity in PCB with 2.5D® technology

1400~
Employees

20+
Years experience

Automotive
Technology focus

AT&S NANJANGUD

Certifications

- ISO 9001:2015
- IATF 16949:2016
- ISO 14001:2015
- ISO 45001:2018
- EN ISO 50001:2018
- ISO/IEC 27001:2013
- UL Listing

CAPABILITIES OVERVIEW*

Build-up	Standard PCBs up to 18 layers HDI up to 4-N-4
Technology	Standard multilayer (4 - 18 layers) Double-sided PCBs with reinforcement HDI PCBs up to 4-N-4 High-Frequency PCBs Cavity in PCB with 2.5D® technology Standard 2 layer PTH
PCB thickness	0.5mm - 2.4mm
Layer count	2 Layer - 18 Layer
Minimum line / spacing	50µm / 50µm
Smallest mechanical drill size	200µm
Smallest laser drill size	100µm
Solder mask	Green / White / Red / Blue / Orange
Surface finish	ENIG OSP Immersion Tin HASL lead-free Electrolytic Hard-Gold Carbon
Production format	18 x 24 Inch 20 x 24 Inch 21 x 24 Inch
Base material	FR4 from mid to high TG Teflon (high frequency material)

Special technology and requirements on request … *

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