### **PCB** Cost drivers



### What drives the cost of a circuit board?



The 'hard costs' and the 'soft costs'.



### Hard cost drivers

- > PCB size
- > Layer count
- > Build/complexity
- > Via treatments
- > Material / panel utilization
- > Track and gap
- > Hole (size & quantity)
- > Additional drilled/routed features

- > Hard gold/thick gold
- > Impedance
- > Excessive tolerances
- > Copper foil weights
- Soldermask, legend/silkscreen, carbon print
- > Surface finishes
- > Materials



If we are able to reduce the size:

#### SUSTAINABILITY IMPACT METER



Size 150\*150mm Price x1 (base price)



Size 300\*300mm ...... Price x4+ ..... ..... 



#### Specific reasons for layer count driving cost:

- Each layer will have to go through the same various processes
- > Cost for each of the inner layers / dry film
- Increased material cost and processing cost
- Developing / Etching / AOI inspection for each inner layer
- > Labor costs
- > Black / brown oxide for each inner layer
- Cost for each piece of pre-preg used between layers
- > Pressing / bonding cycles necessary

If we can reduce the number of layers:

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- 1 > 2 layer +45%
- 2 > 4 layer +40-45%
- 4 > 6 layer +35-40%
- 6 > 8 layer +30-35%
- 8 > 10 layer +25-30%
- 10 > 12 layer +25-30%
- 12 > 14 layer +15-20%

The figures above are average cost adders based upon a cross section of factories. As such these figures shall only be considered as a guide or point of reference.



## HARD COST DRIVERS Build / Complexity

If we are able to design a less complex board:



10L PCB	Base price
Layer of microvia <b>(1+8+1)</b>	+ 40 - 70%
Buried via and microvia (1+8b+1)	+ 80 - 120%
Buried via and microvia with copper fill	+ 120 - 140%





If we are able to reduce or eliminate via treatments:

#### SUSTAINABILITY IMPACT METER



#### Via treatment cost impact

Soldermask covered (Tented)	+0%
Soldermask plug	+1-5%
Type VI	+5-10%
Type VII Nonconductive resin	+7-12%
Type VII Conductive resin	<b>20+%</b> , subject to material MOV





### Material / panel utilization – Example 1

If we make the best use of space on the panel:





**Panelization 1** 



**Panelization 2** 



**Panelization 3** 



### Material / panel utilization – Example 2

If we make the best use of space on the panel:

#### SUSTAINABILITY IMPACT METER





#### **Panelisation 1**

Panel option 1 = 1 panel of 9 circuits, 40mm x 40mm, 10mm carrier rail on 4x sides. Route gap 2.4mm between all circuits Total Panel size =  $304.15 \text{ mm}^2$ 



#### **Panelisation 2**

Panel option 2 = 5mm carrier rail on 2x sides. Route gap 2.4mm between all circuits, Total Panel size = 215.54mm<sup>2</sup> Material reduction = **29%** 



#### **Panelisation 3**

Panel option 3 = 5mm carrier rail on 2x sides. Score lines between all circuits. Total Panel size = 156.00mm<sup>2</sup> Material reduction = **49%** 



#### How does this influence the design and cost?

- > Length of fine line tracks
- > Copper weight / base foil
- > Exposure units
- > Etching methods
- > Handling methods
- > Type of clean room
- > Additive processing vs traditional imaging

If we are able to decrease the amount of smaller/finer traces and spaces:









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#### SUSTAINABILITY IMPACT METER



Fine features should be used sparingly, if you don't need an entire layer to be fine featured only have as much miniaturization as needed.





### HARD COST DRIVERS Hole (size & quantity)

This graphic shows two mechanical drill bits, the smaller having a shorted flute which is the part of the bit that does the actually drilling. If we are able to reduce the number of holes and increase the size:

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38.2 mm (1½")



### HARD COST DRIVERS Additional drilled/routed features

If we are able to reduce the amount of drilled/routed features, or the size:



- > Counter bores
- > Countersinks
- > Backdrilling
- > Controlled depth milling
- > Double sided routing processes.





## HARD COST DRIVERS Hard gold / thick gold

### Examples of common cost adders for hard/thick gold:

- > Extra dry film process
- Additional space necessary for tracks to connect necessary areas
- Less panel utilization with boards with slot-in contacts

If we can decrease the amount of hard and/or thick gold:







- Controlled impedance is a cost driver because it demands very specific controls on line width and spacing along with the dielectric spacing. The production panel must have extra space available for the testing coupons and the actual testing of the coupons via Time Domain Reflectometer test (TDR) is a nonstandard process requiring labor.
- This graphic illustrates some common track structures for impedance variables along with the variable type.

If we can reduce impedance needed:







### **Excessive tolerances**

- > Annular rings below 150µm
- > Outline dimensions tighter than +/- 0.10mm
- > Tracks smaller than 100µm
- > Gaps below 100µm
- > All hole sizes +/- 0.05mm
- > Aspect ratio above 1:8
- > Impedance tighter than +/-10%
- > Line width tolerance tighter than IPC standard

If we are able to eliminate unneeded excessive tolerances:





### **Copper foil weights (thickness)**

If we are able to reduce the amount of copper:

#### SUSTAINABILITY IMPACT METER





Ref copper weights IPC-6012!



### HARD COST DRIVERS Soldermask, legend / silkscreen, carbon print

- Each one is a separate screen print / cure operation
- Cost can be in the region of 2-5% extra dependent upon technology
- Specific soldermask types and colors (high chemical resistance, or blue soldermask for example) can also add more to the price due to material cost, complexity of application or available factory capability.
- > Thick soldermask requirements or heavy copper may require multiple coats increasing labor and throughput.

If we are able to eliminate or reduce specialized solder mask requirement and/or legend silkscreen:







If we are able to use more common surface finishes:



Туре	2-Layer	12-Layer
OSP	0%	0%
HASL	0%	0%
LF HASL	0 - 4%	0 - 1%
Imm Ag	18%	4%
Imm Sn	18%	4%
ENIG	28%	6%
ENEPIG	By quote	By quote





If we are able to use more common base materials:





### Soft cost drivers

- > Under specification
- > Over specification
- > Reliability
- Lead times
- > Transportation costs
- > Lack of knowledge, communication, willingness

## SOFT COST DRIVERS Under specification

#### Some typical examples of missing information:

- > Contour detail
- > Lack of detail regarding PTH vs. NPTH designations
- > Surface finish not specified
- > Copper thickness
- > Base material information not provided
- > Soldermask color
- > Thickness of finished board
- > Missing Gerber files
- > Etc...

If we specify more clearly:

GOOD







#### **Examples of over-specification:**

- > Long specification, takes time to understand
- References to specifications not widely used, such as DIN, BS, IEC etc.
- Over specification can lead to contradictory information
- Over specification can lead to excessively high demands / reliability classification despite purpose

If we have too much or unnecessary information:







To be able to fulfil all demands in accordance IPC class 3, the following three major points must be controlled:

- > **Design:** a tight design might drive the cost or even make it impossible to fulfil the demands.
- Process control: a 'serious' factory will have very stable and well-controlled processes.
- Verification: the verification on a product level for IPC class 3 is extremely time-consuming and should really only be applied for the most demanding of products.

If we design to IPC Class needed rather than Class III which is not needed often:





If we are able to manage with longer lead times:

#### SUSTAINABILITY IMPACT METER



#### Lead time influence on cost





### SOFT COST DRIVERS Transportation costs

If we are able to choose various freight methods:

#### SUSTAINABILITY IMPACT METER





Transportation can be a varied sustainability driver. Expedited freight methods typically have a larger carbon footprint than slower methods.





# Lack of knowledge, communication, willingness

It is very common that bad design, unsuitable material, wasteful panel layouts, etc. is built in at an early stage due to a lack of knowledge, communication with the volume provider or willingness to challenge 'the current way.'

When faced with critical time-to-market situations, it is all too easy to say: "it doesn't matter, this is just the prototype, we can look at or fix this later..."

This can lead to delays or problems when the build gets to volume production. NCAB recommends working with our Field Application Engineers, at the earliest design stages, in order to optimize the design. If we are able to communicate with the experts from the start of the design phase:







### **PCB Cost Drivers** – summary



Customer Electrical Engineer Customer Mechanical Engineer CAD layout Bureau EMS company

NCAB Group

